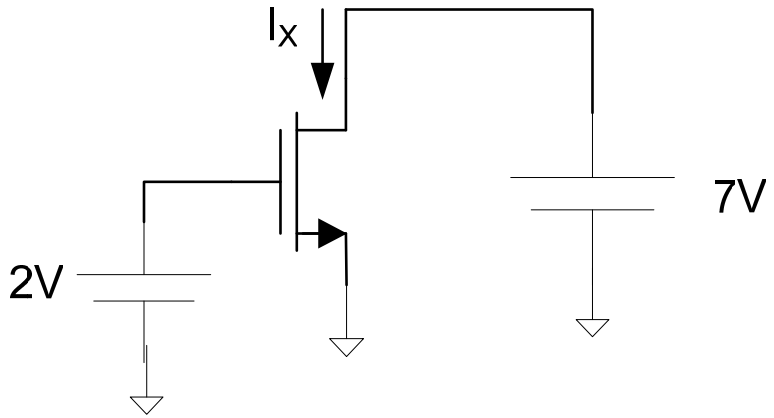
EE 230
Lecture 31

THE MOS TRANSISTOR

Model Simplifcations

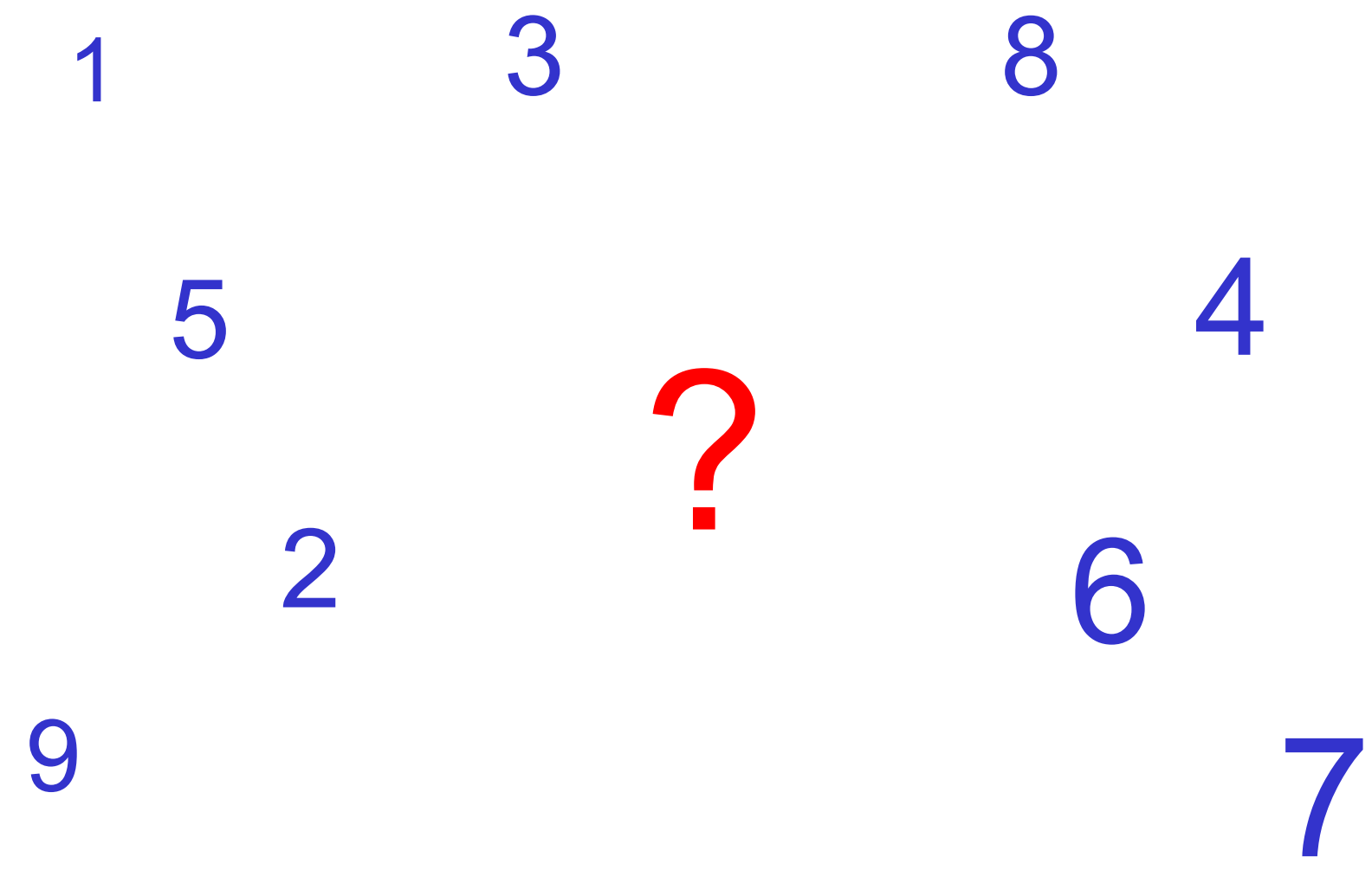
THE Bipolar Junction TRANSISTOR

Quiz 31

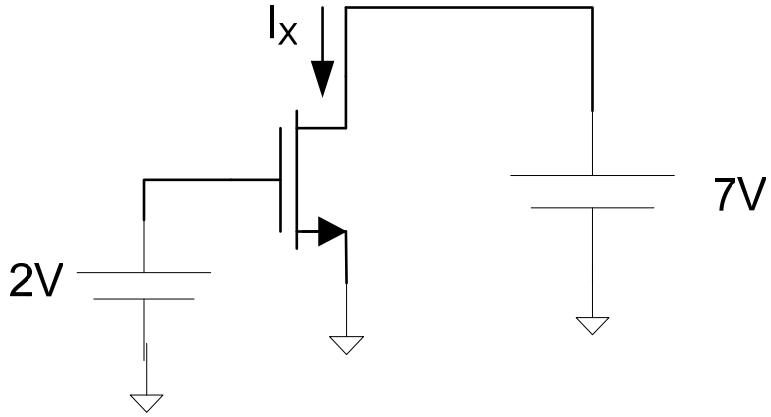


Determine I_X. Assume W=100u, L=2u, V_T=1V, $uC_{OX}=10^{-4}A/V^2$, $\lambda=0$

And the number is ?



Quiz 31 (solution)



Determine I_X. Assume W=100u, L=2u, V_T=1V, $uC_{OX}=10^{-4}A/V^2$, $\lambda=0$

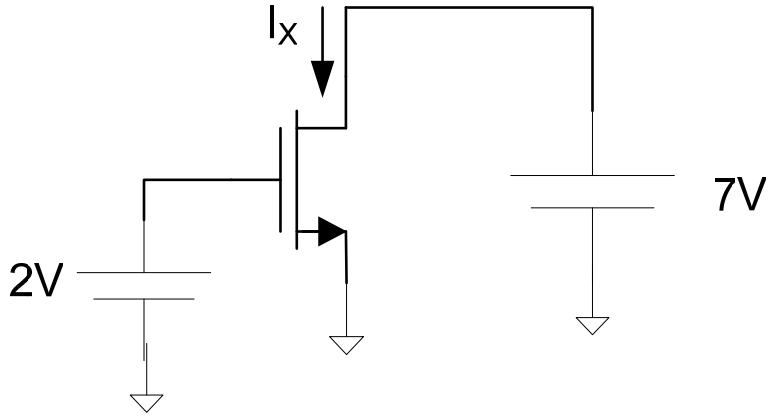
$$I_G = 0$$

$$I_D = \begin{cases} 0 & V_{GS} \le V_T \quad \leftarrow \text{Cutoff} \\ \mu C_{OX}\frac{W}{L}\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_T \quad V_{DS} < V_{GS}-V_T \quad \leftarrow \text{Triode} \\ \mu C_{OX}\frac{W}{2L}\left(V_{GS}-V_T\right)^2 \bullet \left(1+\lambda V_{DS}\right) & V_{GS} \ge V_T \quad V_{DS} \ge V_{GS}-V_T \quad \leftarrow \text{Saturation} \end{cases}$$

Guess Saturation:

$$I_D = \mu C_{OX}\frac{W}{2L}\left(V_{GS}-V_T\right)^2 \qquad V_{GS} \ge V_T \qquad V_{DS} > V_{GS}-V_T$$

Quiz 31 (solution)



Determine I_X. Assume W=100u, L=2u, V_T=1V, $uC_{OX}=10^{-4}A/V^2$, $\lambda=0$

Guess Saturation:

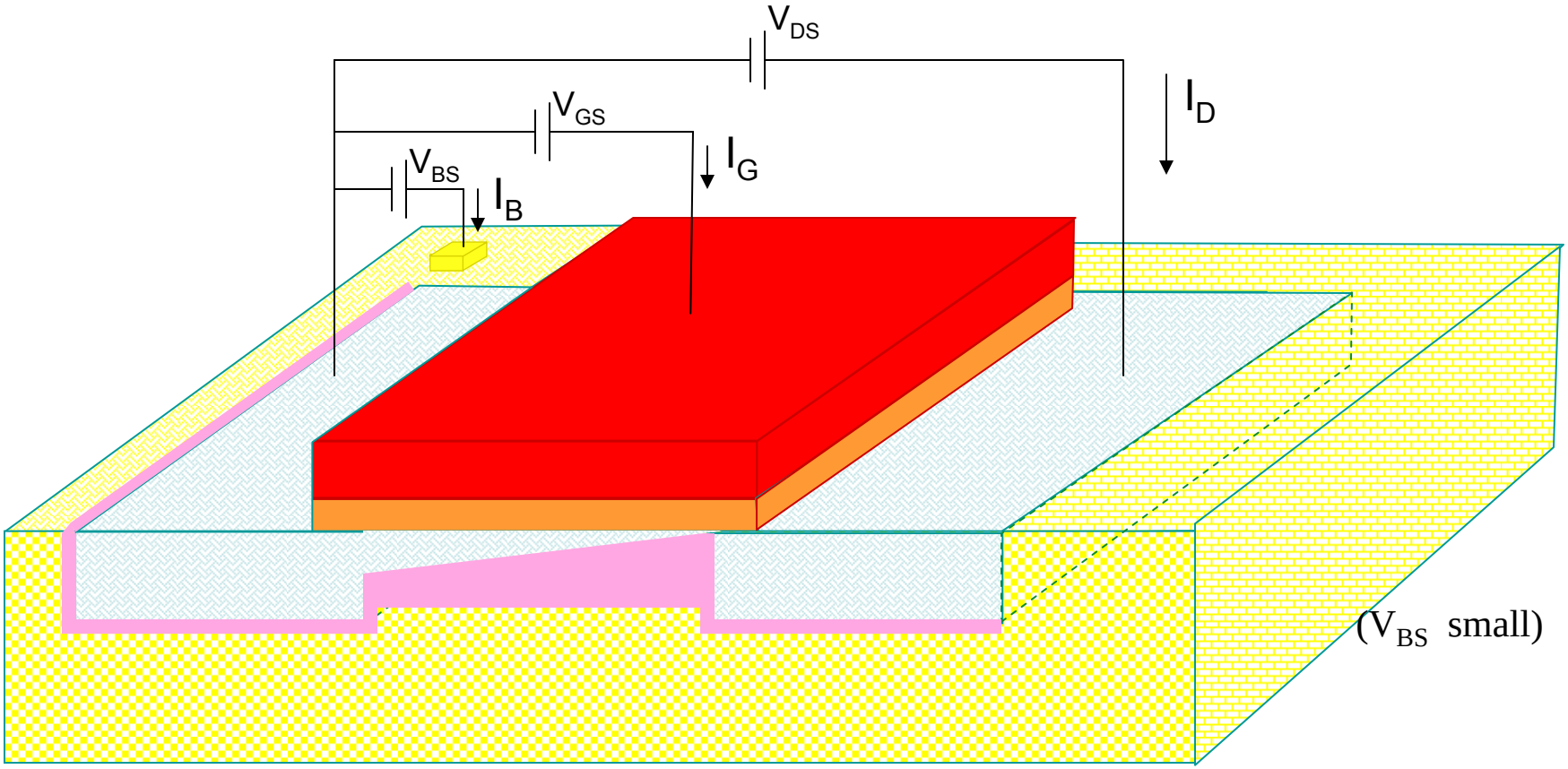
$$I_D = \mu C_{OX}\frac{W}{2L}\left(V_{GS}-V_T\right)^2 \qquad V_{GS} \geq V_T \qquad V_{DS} > V_{GS}-V_T$$

$$I_D = 10^{-4}\frac{100u}{2\bullet 2u}\left(2-1\right)^2 \qquad 2V \geq 1V \qquad 7V > 2V - 1V$$

$$I_D = 2.5mA$$

Review from Last Time:

n-Channel MOSFET Operation and Model



"Saturation" region of operation

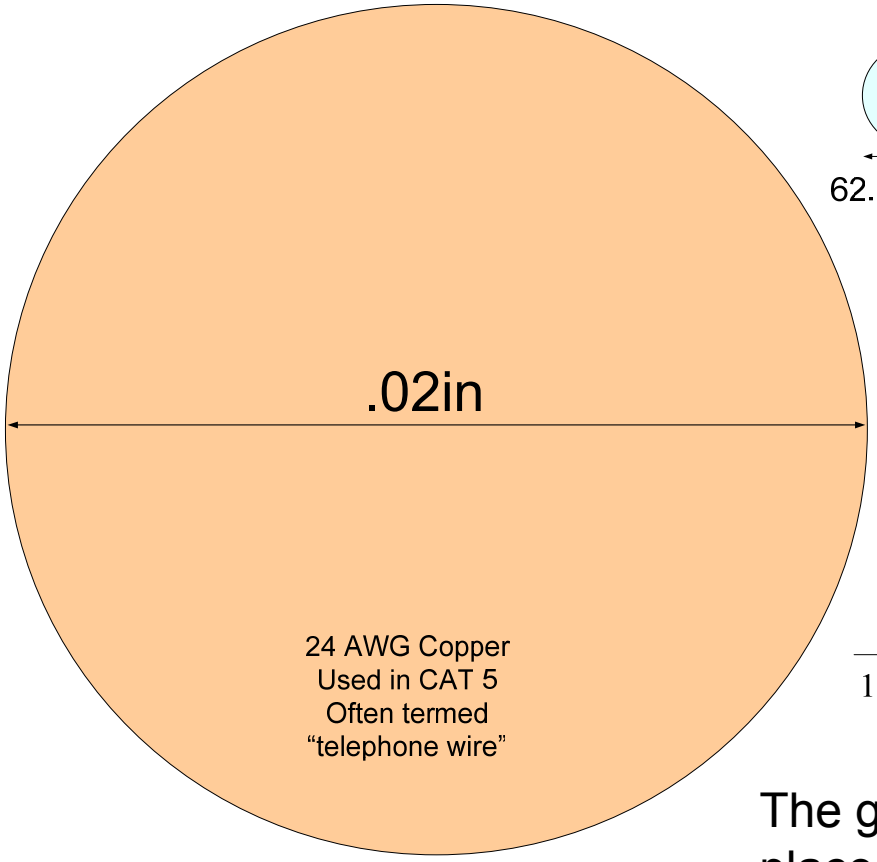
I_D=?
I_G=0
I_B=0

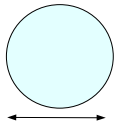
Inversion layer disappears near drain

Saturation first occurs when $V_{DS}=V_{GS}-V_T$

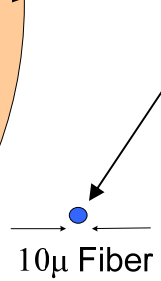
Review from Last Time:

Transistor Size Comparison with 24AWG Copper Cable (Drawn to scale)





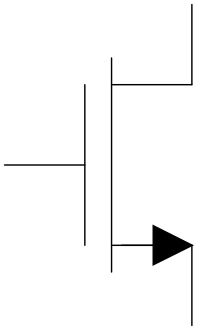
State of Art transistor dimensions about 200 times smaller (lateral) than 10µ fiber

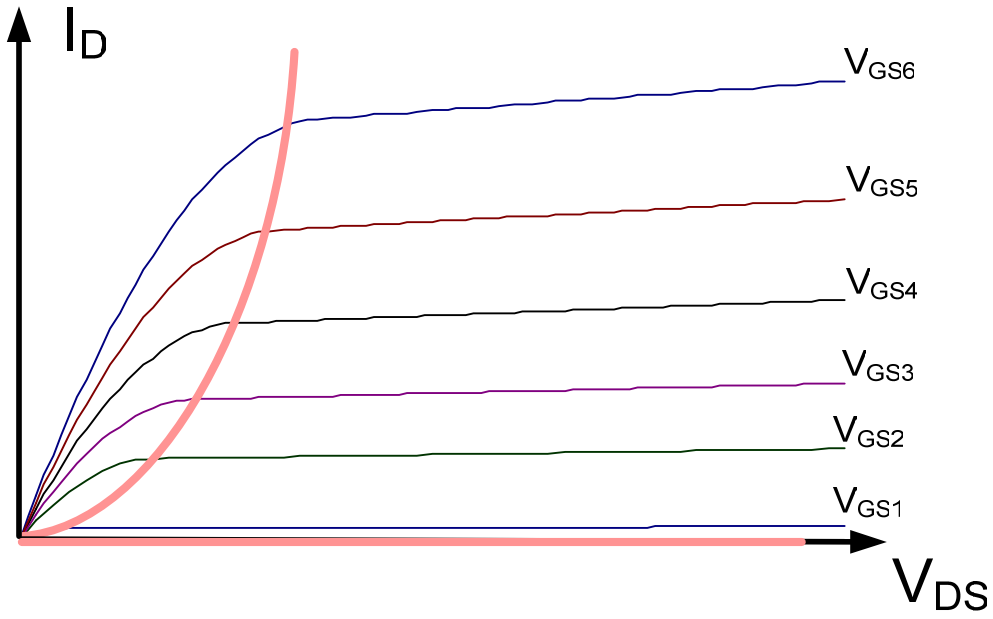


The gates of about 40000 transistors can be placed on the cross-section of this fiber (maybe only 4000 transistors)

Review from Last Time:

MOS Transistors





Standard square-law model

$I_G = 0$

$$I_D = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ \left(\frac{\mu_n C_{OX} W}{L}\right)\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_T \quad V_{DS} \leq V_{GS}-V_T \quad \text{Triode} \\ \left(\frac{\mu_n C_{OX} W}{2L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS}) & V_{GS} \geq V_T \quad V_{DS} > V_{GS}-V_T \quad \text{Saturation} \end{cases}$$

$\mu_n C_{OX} \approx 10^{-4} \, A/V^2$

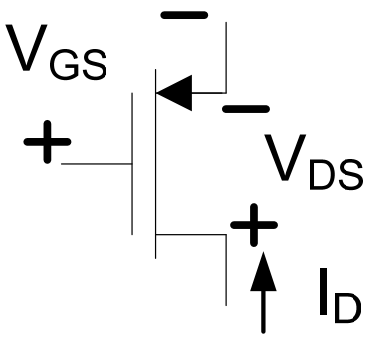
$\lambda \approx .01 V^{-1}$

$V_T \approx 0.5V$ to $3V$

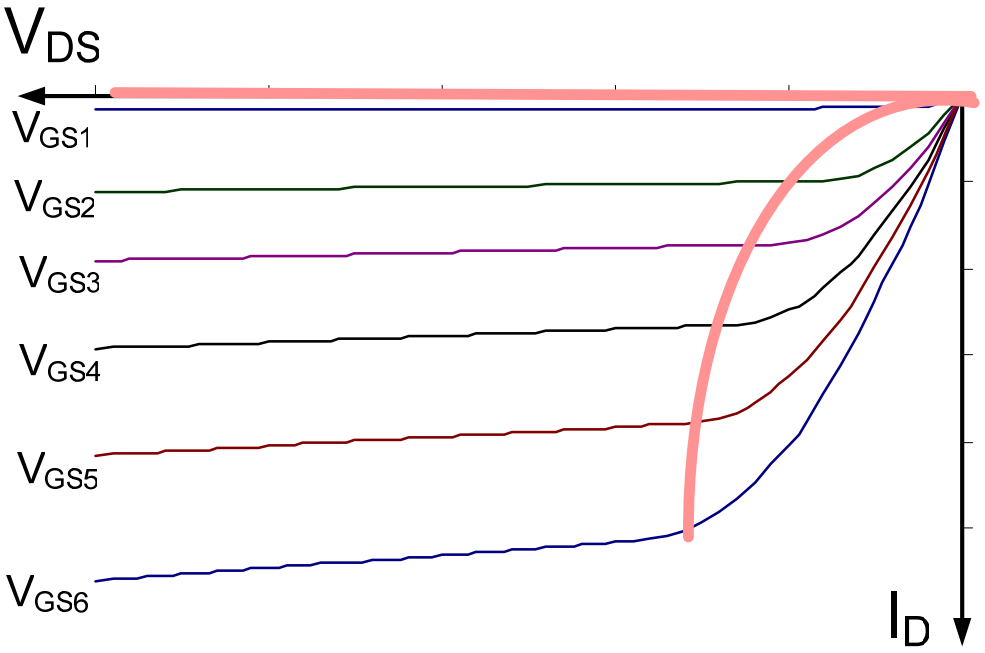
W/L varies by design

Review from Last Time:

MOS Transistors



p-channel MOSFET



Standard square-law model

$$I_G = 0$$

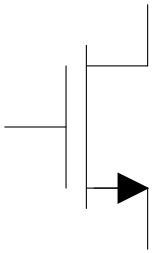
$$I_D = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ -\left(\frac{\mu_p C_{OX} W}{L}\right)\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \le V_T \quad V_{DS} \ge V_{GS}-V_T \quad \text{Triode} \\ -\left(\frac{\mu_p C_{OX} W}{2L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS}) & V_{GS} \le V_T \quad V_{DS} < V_{GS}-V_T \quad \text{Saturation} \end{cases}$$

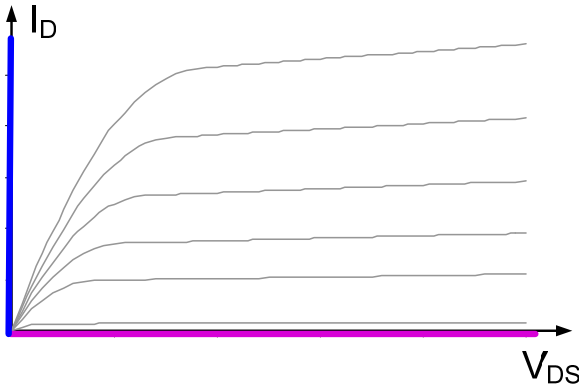
$V_T < 0$
$I_D \le 0$
$V_{DS} \le 0$

Review from Last Time:

MOS Transistor Models

simplifications



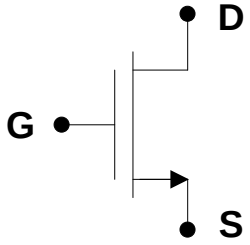


$I_G=0$

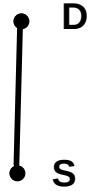
$I_D=0$ $V_{GS}<V_T$ Cutoff

$V_{DS}=0$ $V_{GS} \geq V_T$ Triode

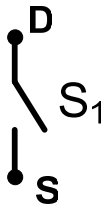
Equivalent Circuit Models



$V_{GS}<V_T$



$V_{GS}>V_T$



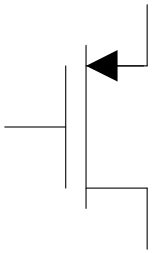
S_1 open for $V_{GS}<V_T$

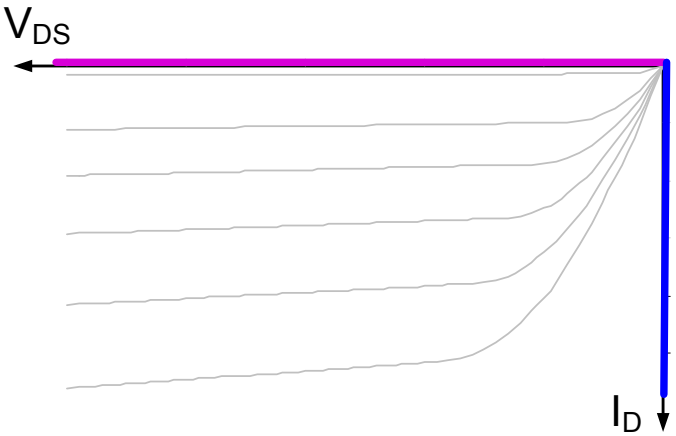
S_1 closed for $V_{GS}>V_T$

Review from Last Time:

MOS Transistor Models

simplifications



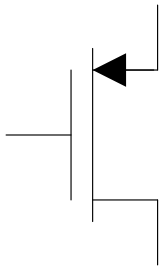


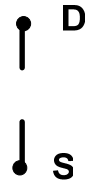
$I_G = 0$

$I_D = 0$ $\quad V_{GS} > V_T$ $\quad$ Cutoff

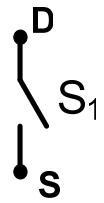
$V_{DS} = 0$ $\quad V_{GS} \leq V_T$ $\quad$ Triode

Equivalent Circuit Models





$V_{GS} > V_T$ $\quad V_{GS} < V_T$



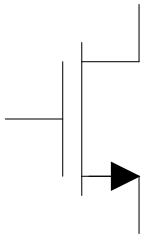
S_1 open for $V_{GS} > V_T$

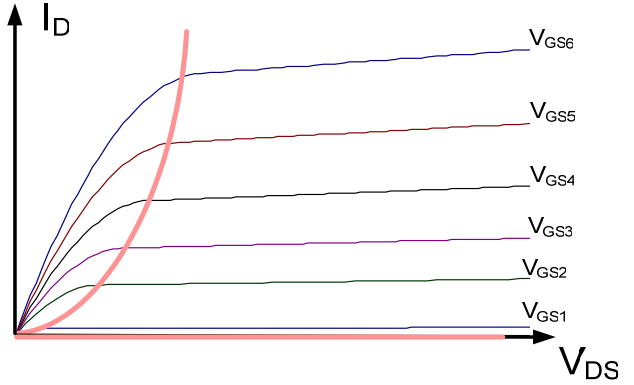
S_1 closed for $V_{GS} < V_T$

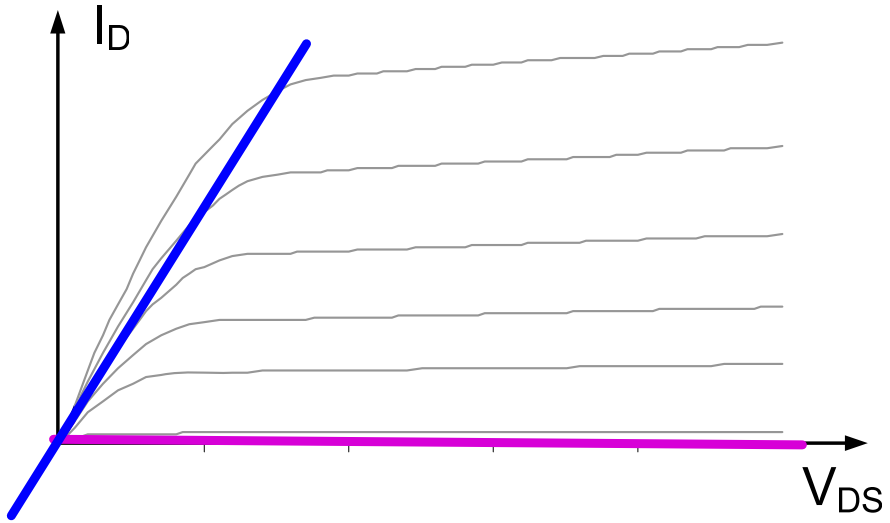
Review from Last Time:

MOS Transistor Models

simplifications







$I_G = 0$

$$I_D = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ V_{DS} / R_{FET} & V_{GS} \geq V_T \quad \text{Triode} \end{cases}$$

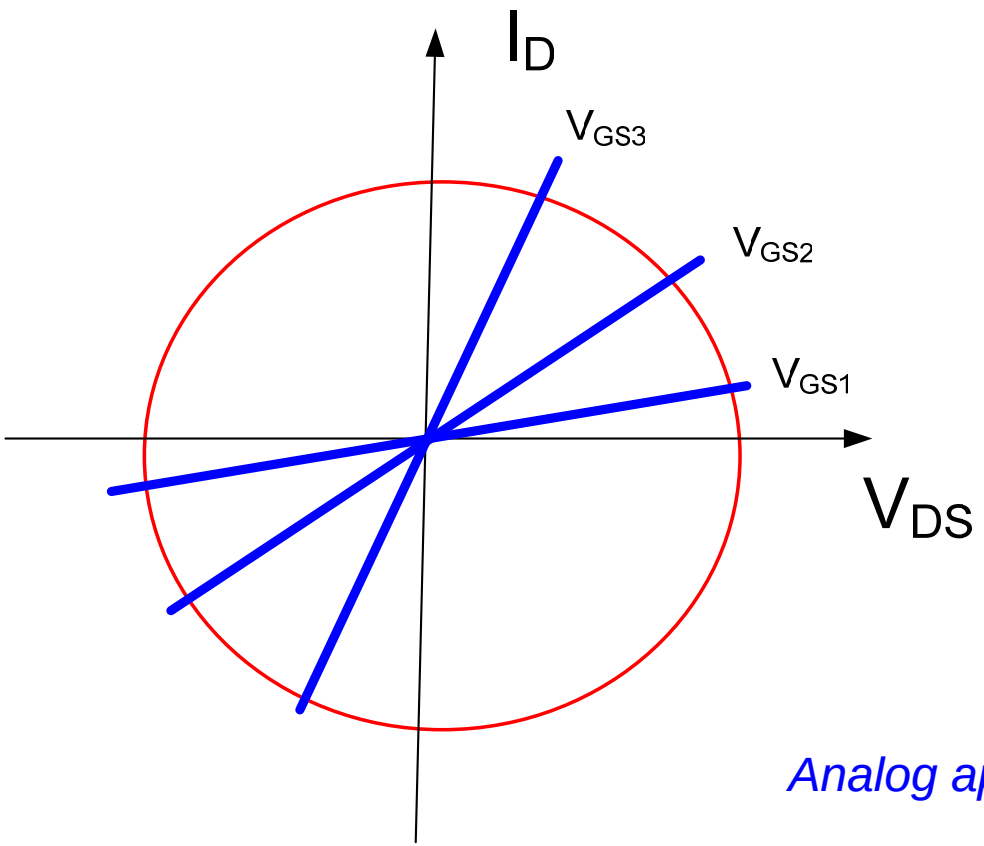
$$R_{FET} \cong \frac{1}{V_{GS} - V_T} \left(\frac{L}{\mu C_{OX} W} \right)$$

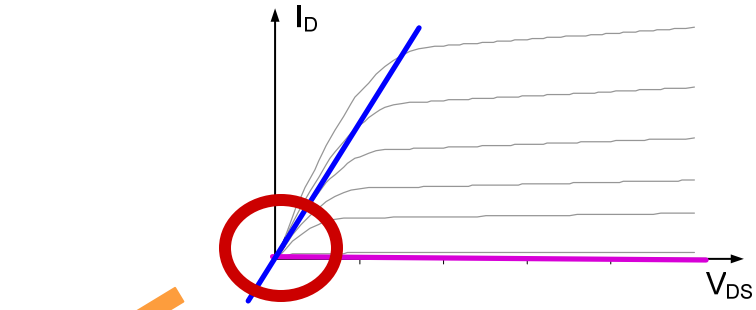
Better Switch-level dc model – *good enough for predicting basic operation of many digital circuits and can be used to predict speed performance if parasitic capacitances are added*

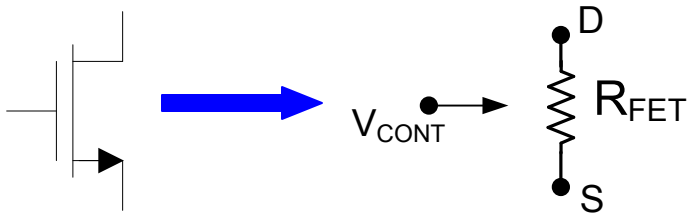
Review from Last Time:

MOS Transistor Models

Voltage Variable Resistor (VVR) operation





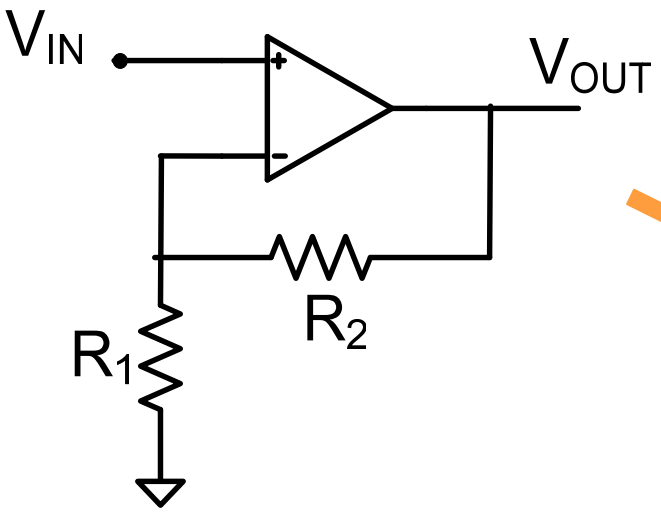


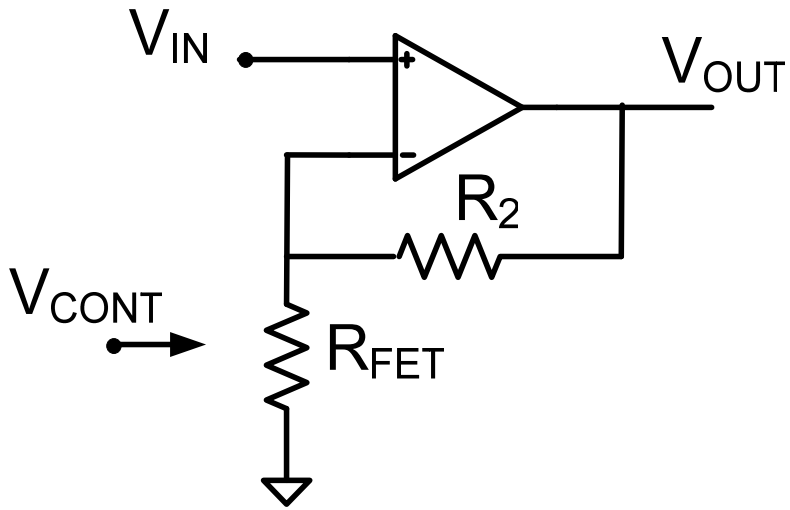
$$R_{FET} \cong \frac{1}{V_{GS}-V_T}\left(\frac{L}{\mu C_{OX} W}\right)$$

Analog application of MOSFET in triode region

Review from Last Time:

Voltage Variable Resistor





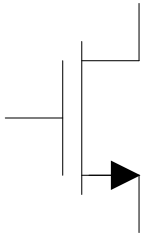
$$A_V = 1 + \frac{R_2}{R_1}$$

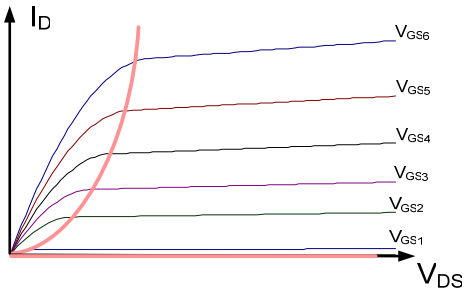
$$A_V = 1 + \frac{R_2}{R_{FET}}$$

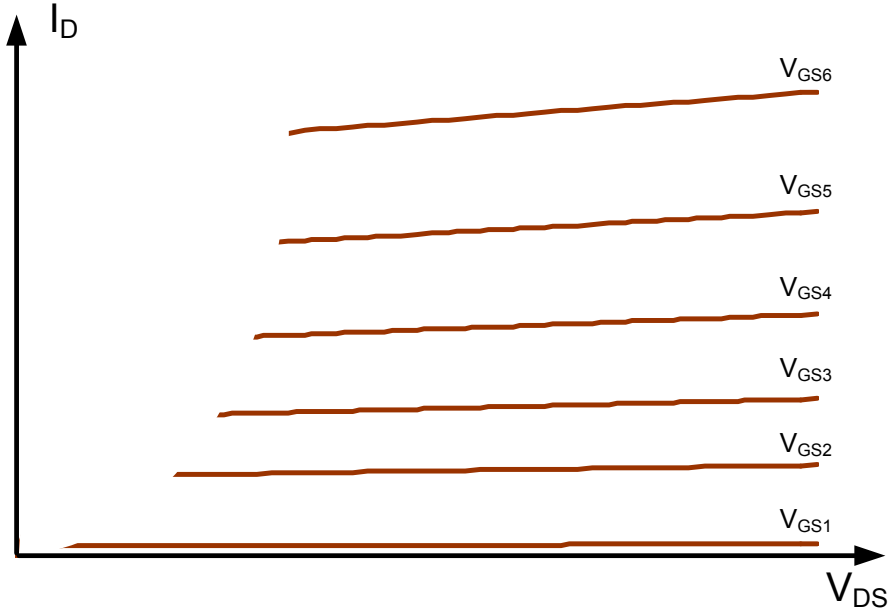
$$R_{FET} \cong \frac{1}{V_{GS} - V_T} \left(\frac{L}{\mu C_{OX} W} \right)$$

Applications include Automatic Gain Control (AGC)

MOS Transistor Models
simplifications







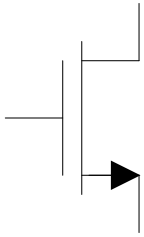
$$I_G = 0$$

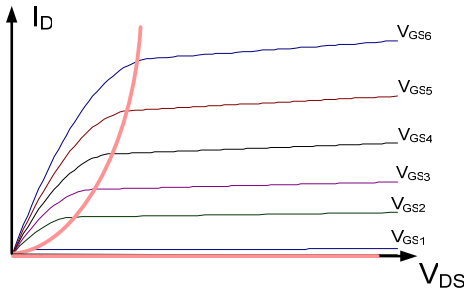
$$I_D = \left(\frac{\mu C_{OX} W}{2L}\right)(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad \textbf{\textit{Saturation}}$$

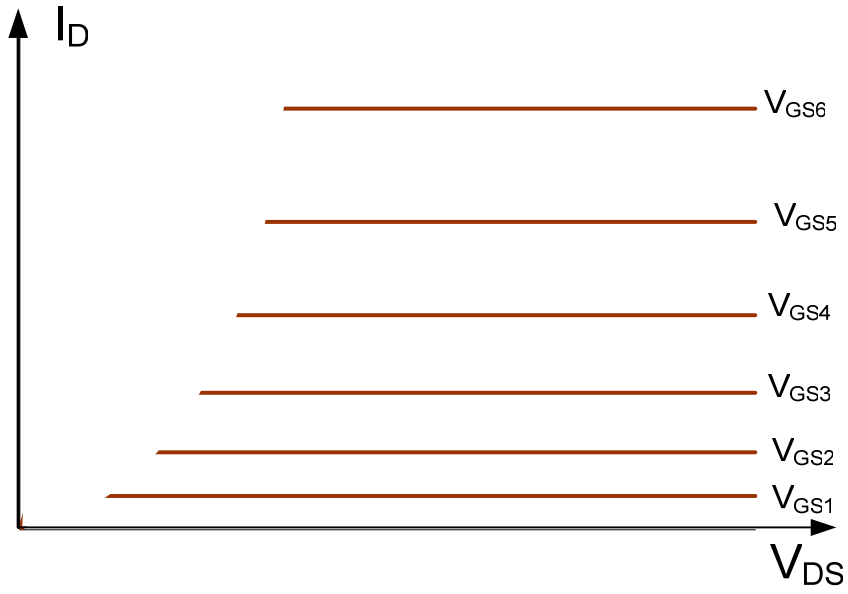
Can often assume $\lambda = 0$

Saturation Region Model – *used for many analog applications*

MOS Transistor Models
simplifications







$$I_G = 0$$

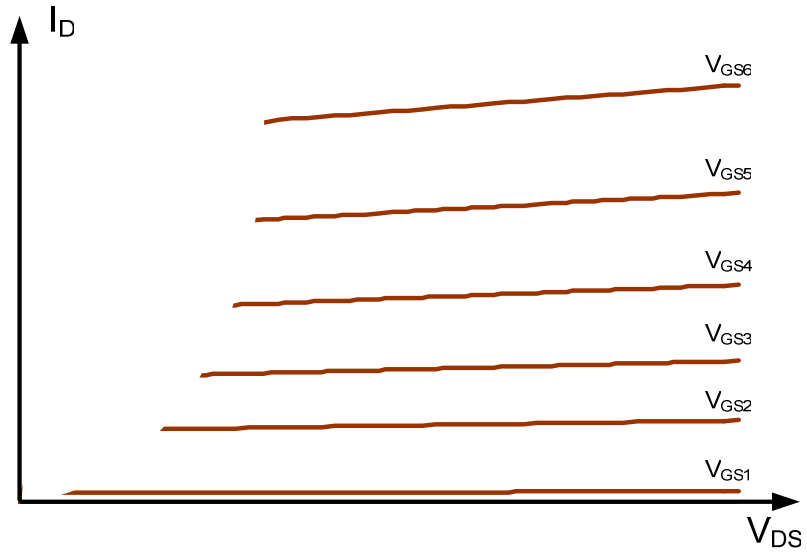
$$I_D = \left(\frac{\mu C_{OX} W}{2L}\right)\left(V_{GS} - V_T\right)^2$$

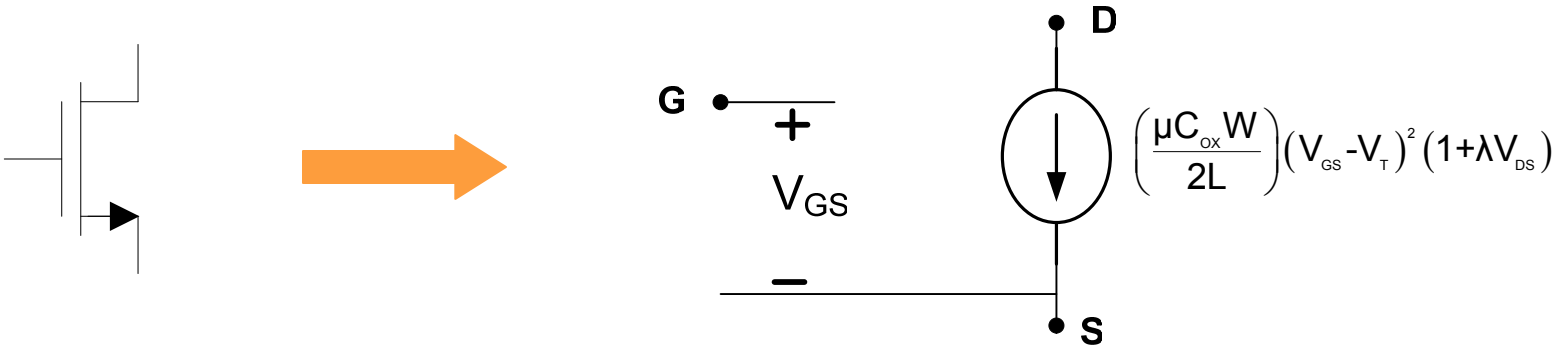
Saturation

With λ=0

Saturation Region Model – *good enough for many analog applications*

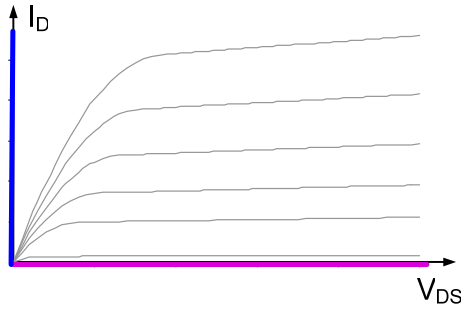
MOS Transistor Models
simplifications

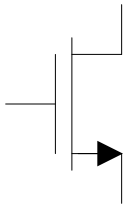


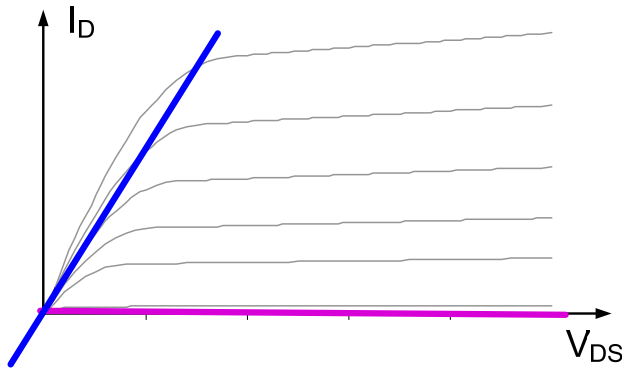


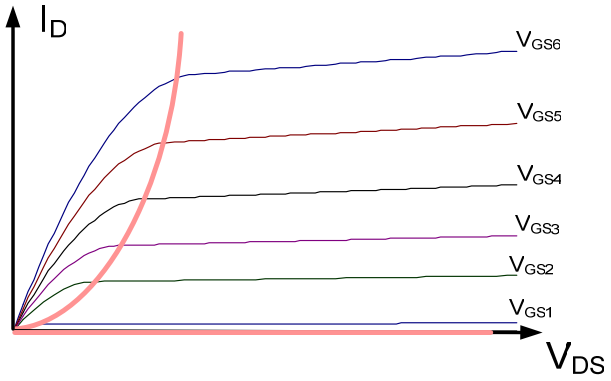
Saturation Region Model – *good enough for many analog applications*

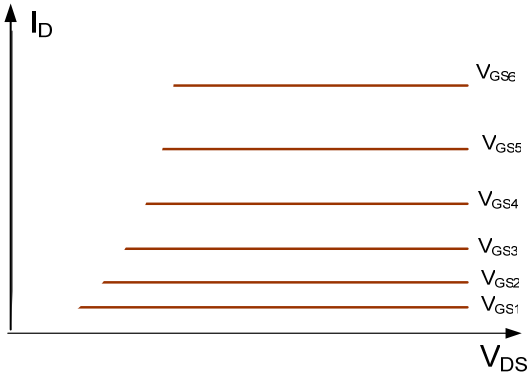
MOS Transistor Models (Summary)

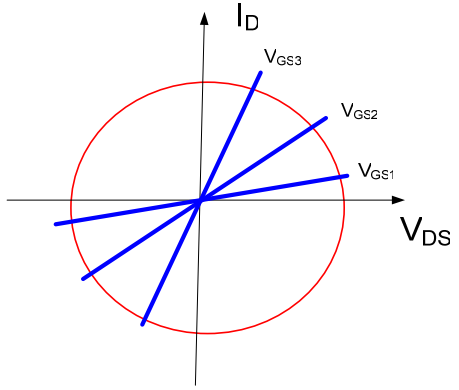




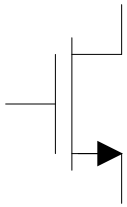


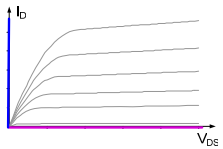


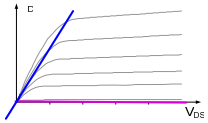


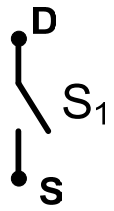


MOS Transistor Models (Summary)



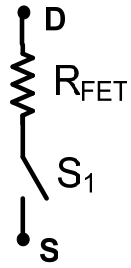






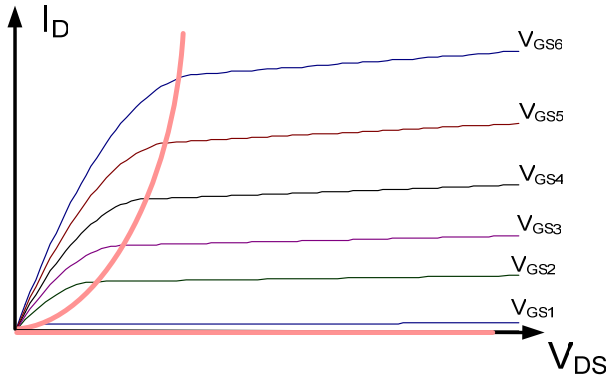
S_1 open for $V_{GS}<V_T$

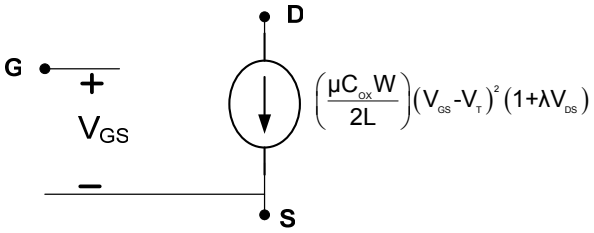
S_1 closed for $V_{GS}>V_T$

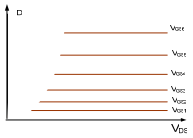


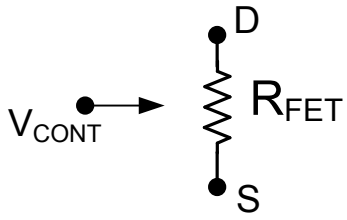
S_1 closed for $V_{GS}>V_T$

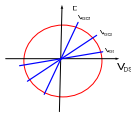
S_1 open $V_{GS}<V_T$



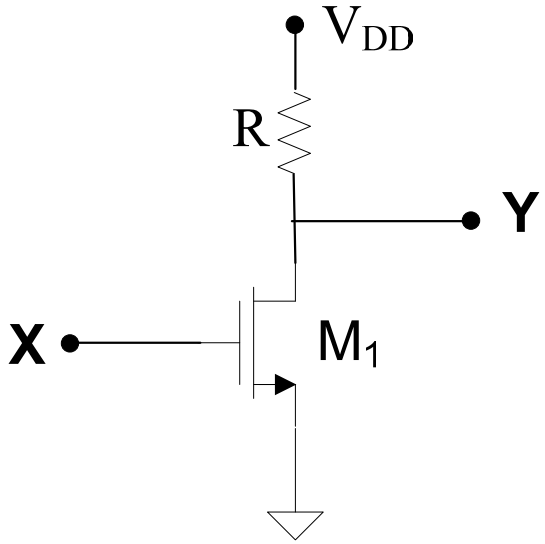








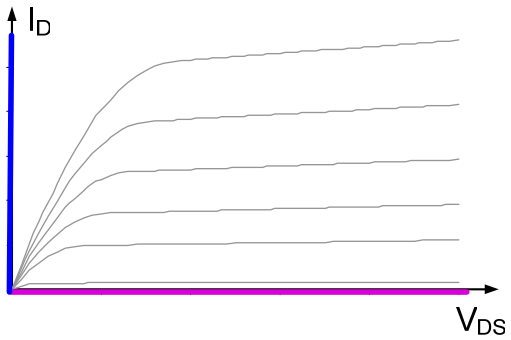
MOS Transistor Applications (Digital Circuits)



Assume "1" ~ $V_H = V_{DD} > V_T$

Assume "0" ~ $V_L = 0V < V_T$

MOSFET Model

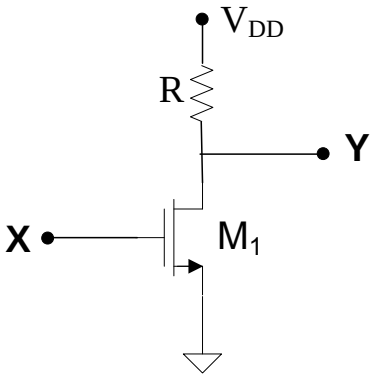


$I_G = 0$

$I_D = 0$	$V_{GS} < V_T$	Cutoff
$V_{DS} = 0$	$V_{GS} \geq V_T$	Triode

Assume $V_T \sim V_{DD}/5$

MOS Transistor Applications (Digital Circuits)



Assume "1" ~ $V_H = V_{DD} > V_T$

Assume "0" ~ $V_L = 0V < V_T$

$I_D = 0$ $V_{GS} < V_T$ Cutoff

$V_{DS} = 0$ $V_{GS} \geq V_T$ Triode

Assume $V_T \sim V_{DD}/5$

If "1"~ **X**= V_{DD}, V_{DS}= 0V so Y = 0V ~ *"0"*

If "0"~ **X**= 0V, I_D= 0A so Y =V_{DD}-I_DR = V_{DD} ~ "1"

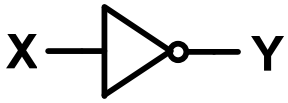
So this circuit performs as a Boolean inverter

Assume "0" ~ $V_L < V_T$

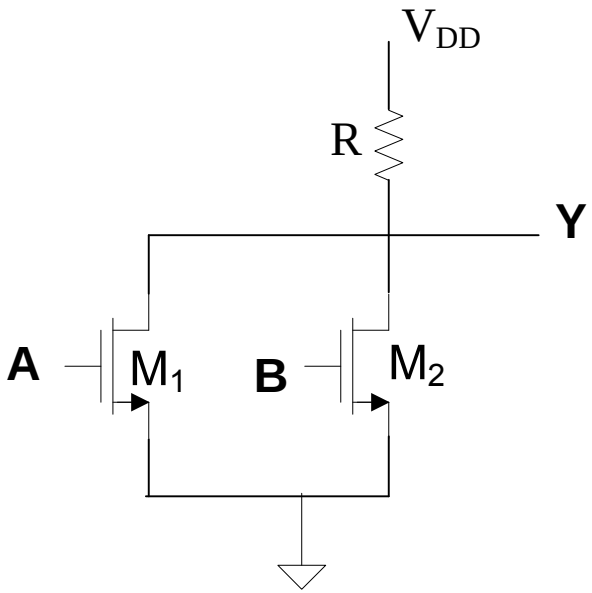
Assume "1" ~ $V_H > V_T$

X	Y
0	1
1	0

Truth Table



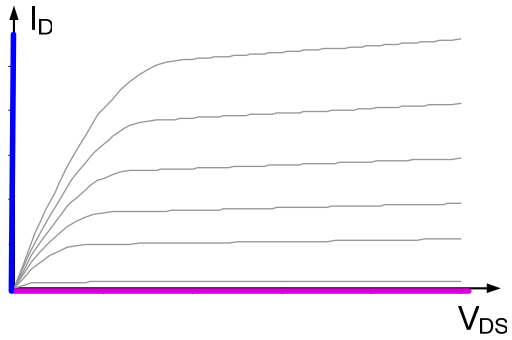
MOS Transistor Applications (Digital Circuits)



Assume "1" ~ $V_H = V_{DD} > V_T$

Assume "0" ~ $V_L = 0V < V_T$

MOSFET Model

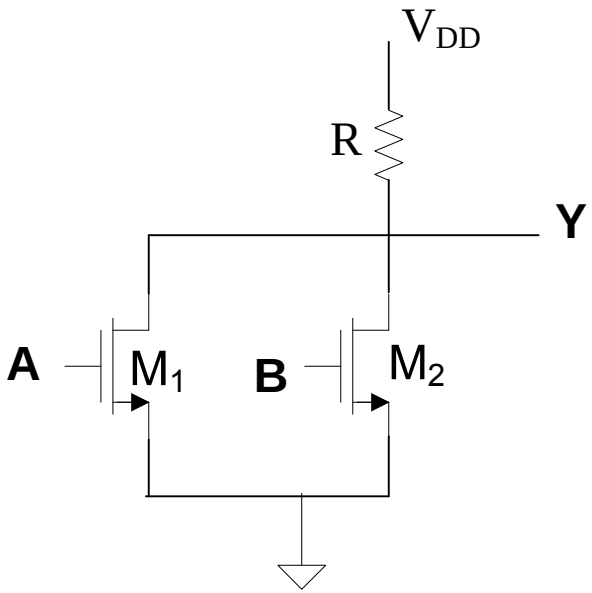


$I_G = 0$

$I_D = 0$	$V_{GS} < V_T$	Cutoff
$V_{DS} = 0$	$V_{GS} \geq V_T$	Triode

Assume $V_T \sim V_{DD}/5$

MOS Transistor Applications (Digital Circuits)



Assume "1" ~ $V_H = V_{DD} > V_T$

Assume "0" ~ $V_L = 0V < V_T$

$I_D = 0$ $V_{GS} < V_T$ Cutoff

$V_{DS} = 0$ $V_{GS} \geq V_T$ Triode

Assume $V_T \sim V_{DD}/5$

If "1"~ **A**= V_{DD}, "1"~ B= V_{DD}, $V_{DS1}=V_{DS2}= 0V$ so Y = 0V ~ *"0"*

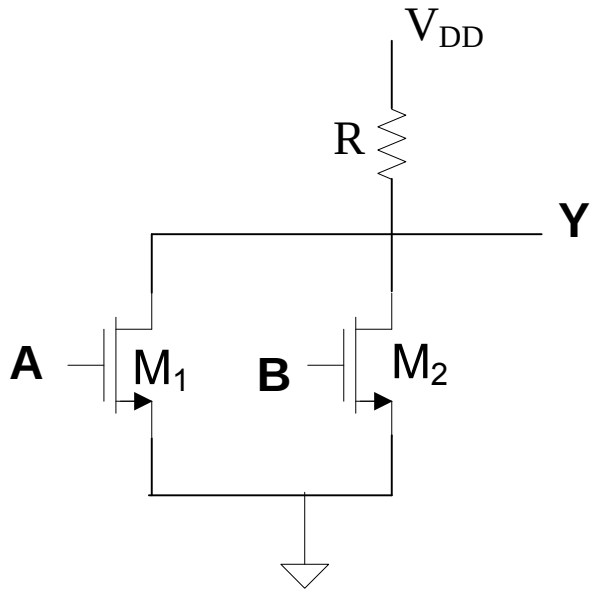
If "1"~ **A**= V_{DD}, "0"~ B= 0V, $V_{DS1}= 0V$ *(and $I_{D2}=0A$)* so Y = 0V ~ *"0"*

If "0"~ **A**= 0V, "1"~ B= V_{DD}, $V_{DS2}= 0V$ *(and $I_{D1}=0A$)* so Y = 0V ~ *"0"*

If "0"~ **A**= 0V, "0"~ B= 0V, $I_{D2}= 0A$ *and $I_{D1}=0A$* so $I_R=0A$, thus

Y = $V_{DD} = I_R R = V_{DD}$ ~ *"1"*

MOS Transistor Applications (Digital Circuits)



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

If "1"~ **A**= V_{DD}, "1"~ B= $V_{DD,}$ V_{DS1}=V_{DS2}= 0V so Y = 0V ~ *"0"*

If "1"~ **A**= V_{DD}, "0"~ B= 0V, V_{DS1}= 0V *(and* I_{D2}*=0A)* so Y = 0V ~ *"0"*

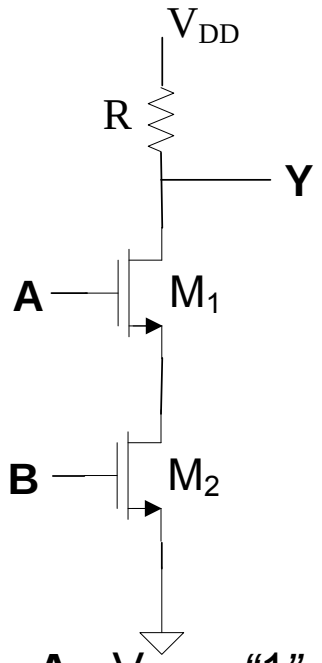
If "0"~ **A**= 0V, "1"~ B= $V_{DD,}$ V_{DS2}= 0V *(and* I_{D1}*=0A)* so Y = 0V ~ *"0"*

If "0"~ **A**= 0V, "0"~ B= 0V, I_{D2}= 0A *and* I_{D1}*=0A* so I_R=0A, thus

Y = V_{DD}= I_RR=V_{DD} ~ *"1"*

2-input NOR Gate

MOS Transistor Applications (Digital Circuits)



Assume "1" ~ $V_H = V_{DD} > V_T$

Assume "0" ~ $V_L = 0V < V_T$

$I_D = 0$ $V_{GS} < V_T$ Cutoff

$V_{DS} = 0$ $V_{GS} \geq V_T$ Triode

Assume $V_T \sim V_{DD}/5$

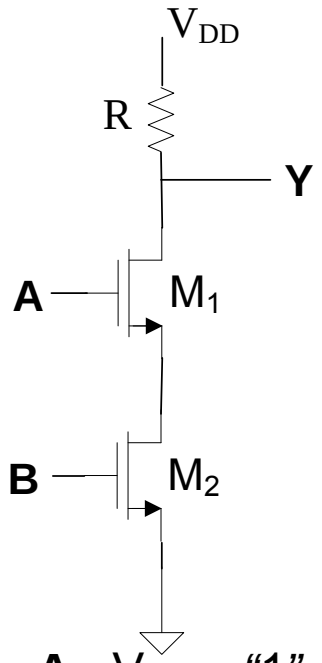
If "1"~ **A**= V_{DD}, "1"~ B= V_{DD}, $V_{DS1}=V_{DS2}= 0V$ so Y =0V ~ *"0"*

If "1"~ **A**= V_{DD}, "0"~ B= 0V, $V_{DS1}= 0V$ and $I_{D2}=0A$ so $I_R=0A$ thus
$Y = V_{DD} - I_R R = V_{DD}$ ~ "1"

If "0"~ **A**= 0V, "1"~ B= V_{DD}, $V_{DS2}= 0V$ and $I_{D1}=0A$ so $I_R=0A$ thus
$Y = V_{DD} - I_R R = V_{DD}$ ~ "1"

If "0"~ **A**= 0V, "0"~ B= 0V, $I_{D1}= 0A$ and $I_{D2}=0A$ so $I_R=0A$ thus
$Y = V_{DD} - I_R R = V_{DD}$ ~ "1"

MOS Transistor Applications (Digital Circuits)



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

If "1"~ **A**= V_{DD}, "1"~ B= V_{DD}, V_{DS1}=V_{DS2}= 0V so Y =0V ~ *"0"*

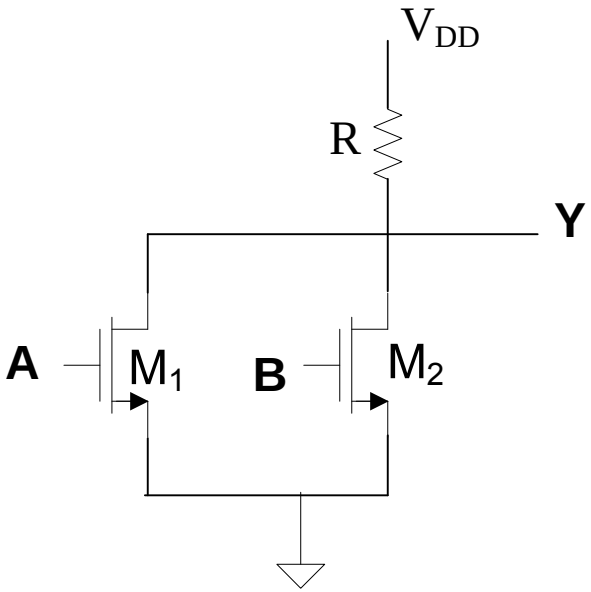
If "1"~ **A**= V_{DD}, "0"~ B= 0V, V_{DS1}= 0V and I_{D2}=0A so I_R=0A thus
Y =V_{DD}-I_RR= V_{DD} ~ "1"

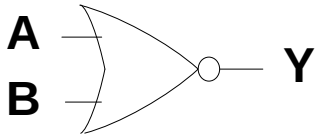
If "0"~ **A**= 0V, "1"~ B= V_{DD}, V_{DS2}= 0V and I_{D1}=0A so I_R=0A thus
Y =V_{DD}-I_RR= V_{DD} ~ "1"

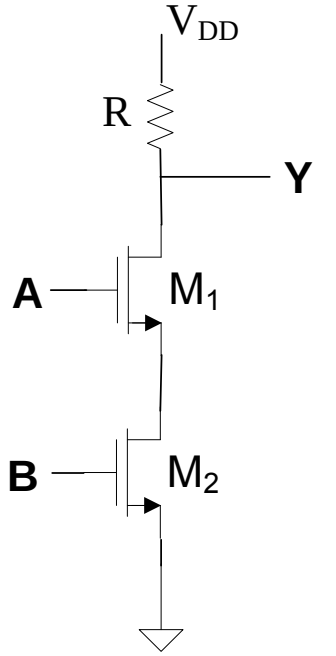
If "0"~ **A**= 0V, "0"~ B= 0V, I_{D1}= 0A and I_{D2}=0A so I_R=0A thus
Y =V_{DD}-I_RR= V_{DD} ~ "1"

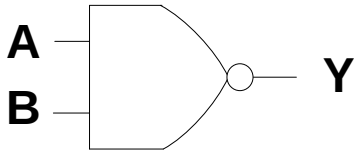
2-input NAND Gate

MOS Transistor Applications (Digital Circuits)



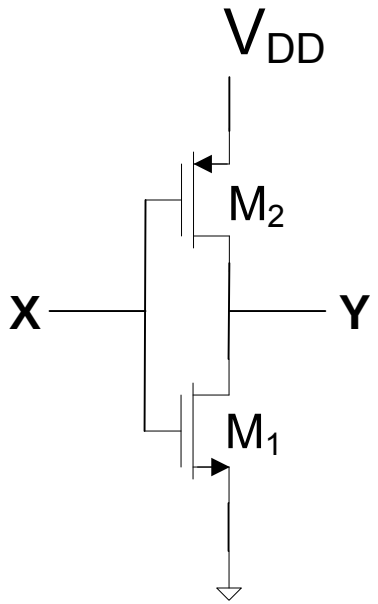






- Can be extended to arbitrary number of inputs
- But the resistor is not practically available in most processes and static power dissipation is too high

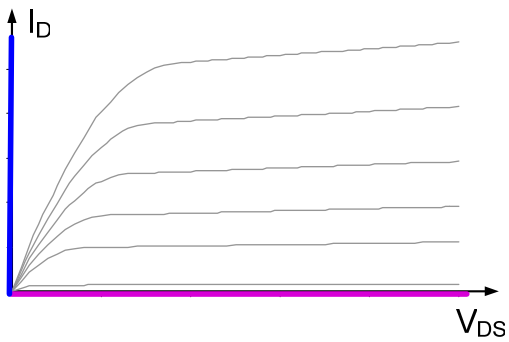
MOS Transistor Applications (Digital Circuits)

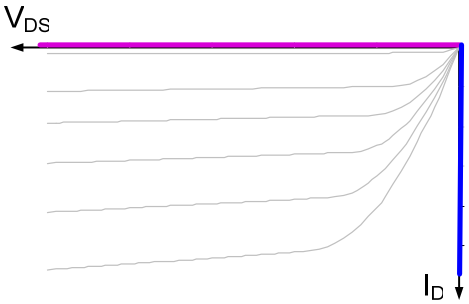


Assume "1" ~ $V_H = V_{DD}$

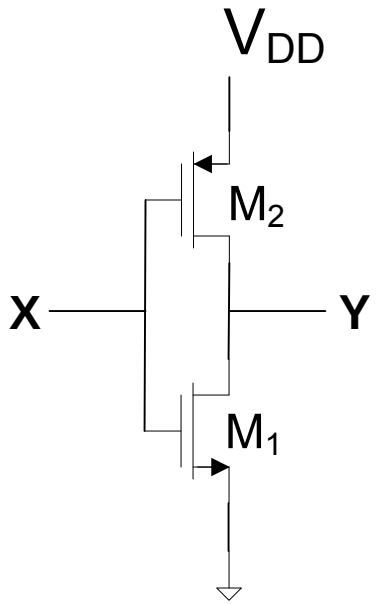
Assume "0" ~ $V_L = 0V$

MOSFET Models





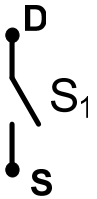
MOS Transistor Applications (Digital Circuits)



Assume "1" ~ $V_H = V_{DD}$

Assume "0" ~ $V_L = 0V$

MOSFET Models

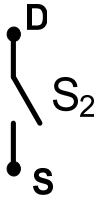


S_1 open for $V_{GS1} < V_{T1}$

S_1 closed for $V_{GS1} > V_{T1}$

Assume $V_{T1} \sim V_{DD}/5$

n-channel device



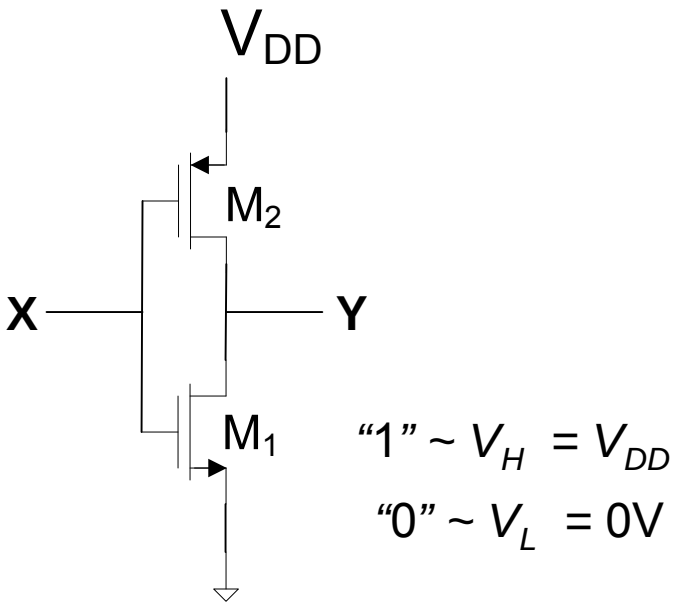
S_2 open for $V_{GS2} > V_{T2}$

S_2 closed for $V_{GS2} < V_{T2}$

Assume $V_{T2} \sim -V_{DD}/5$

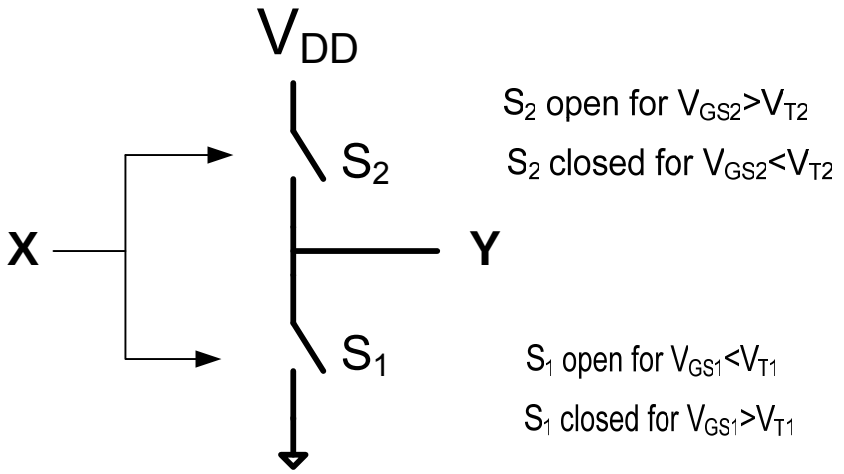
p-channel device

MOS Transistor Applications (Digital Circuits)

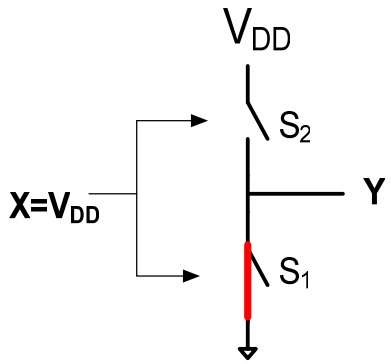


"1" ~ $V_H = V_{DD}$

"0" ~ $V_L = 0V$

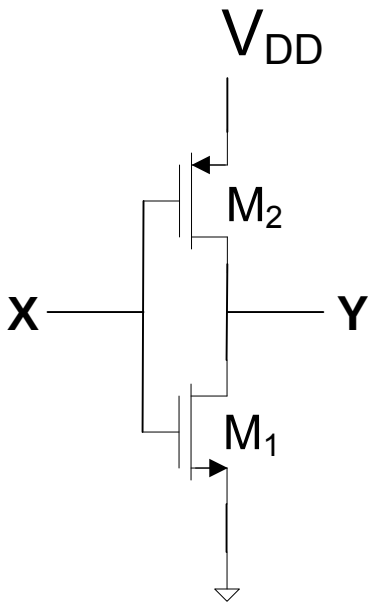


If $X=V_{DD}$, then $V_{GS1}=V_{DD}>V_{T1}$, $V_{GS2}=0 > V_{T2}$ → *S_1 closed, S_2 open*



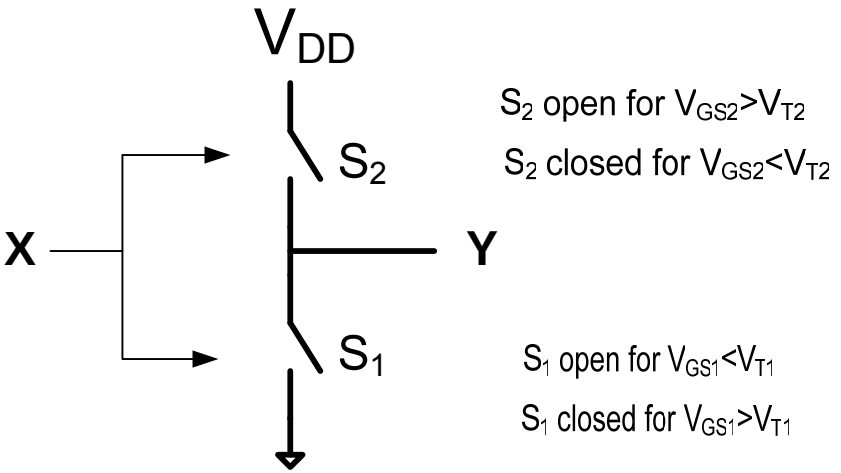
Y = 0V~"0"

MOS Transistor Applications (Digital Circuits)

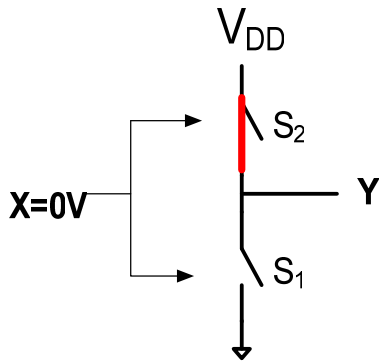


"1" ~ $V_H = V_{DD}$

"0" ~ $V_L = 0V$

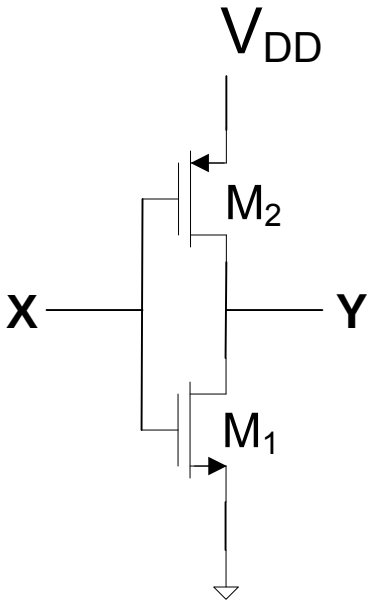


If X=0V , then $V_{GS1}=0V<V_{T1}$, $V_{GS2}=-V_{DD} < V_{T2}$ ➡ *S_2 closed, S_1 open*



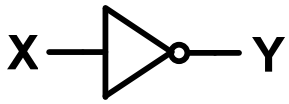
$Y = V_{DD}$~"1"

MOS Transistor Applications (Digital Circuits)



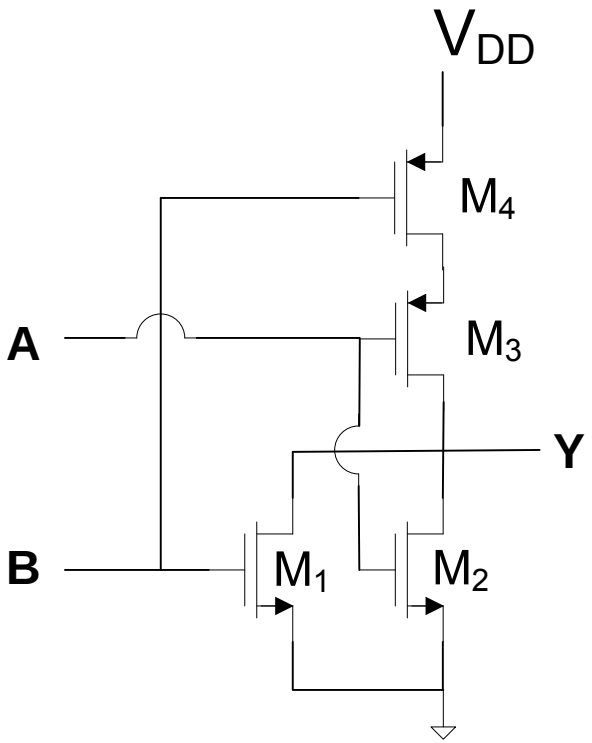
X	Y
0	1
1	0

Truth Table



Performs as a digital inverter

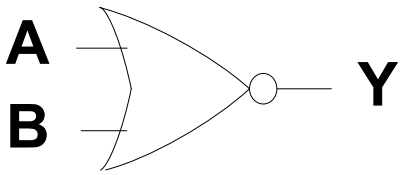
MOS Transistor Applications (Digital Circuits)



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

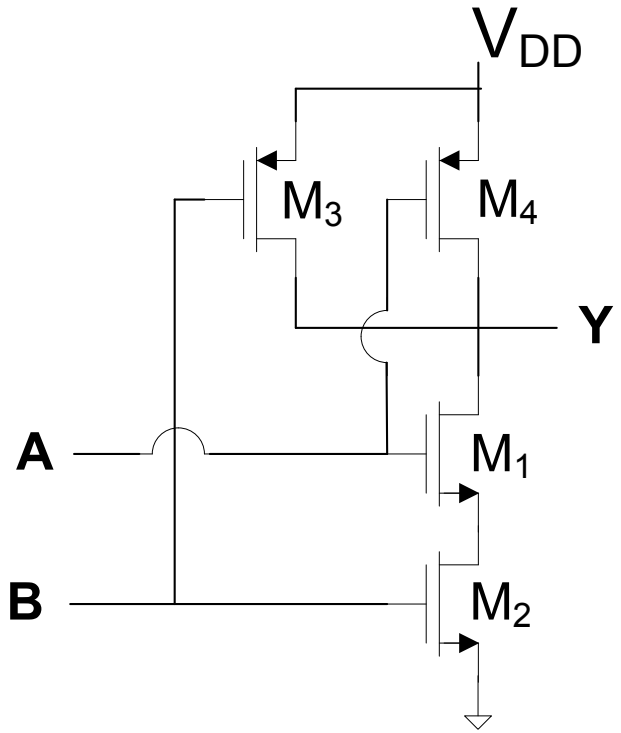
Truth Table

Performs as a 2-input NOR Gate



Can be easily extended to an n-input NOR Gate

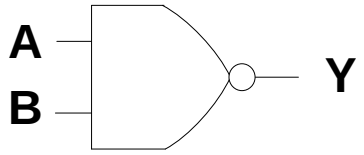
MOS Transistor Applications (Digital Circuits)



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

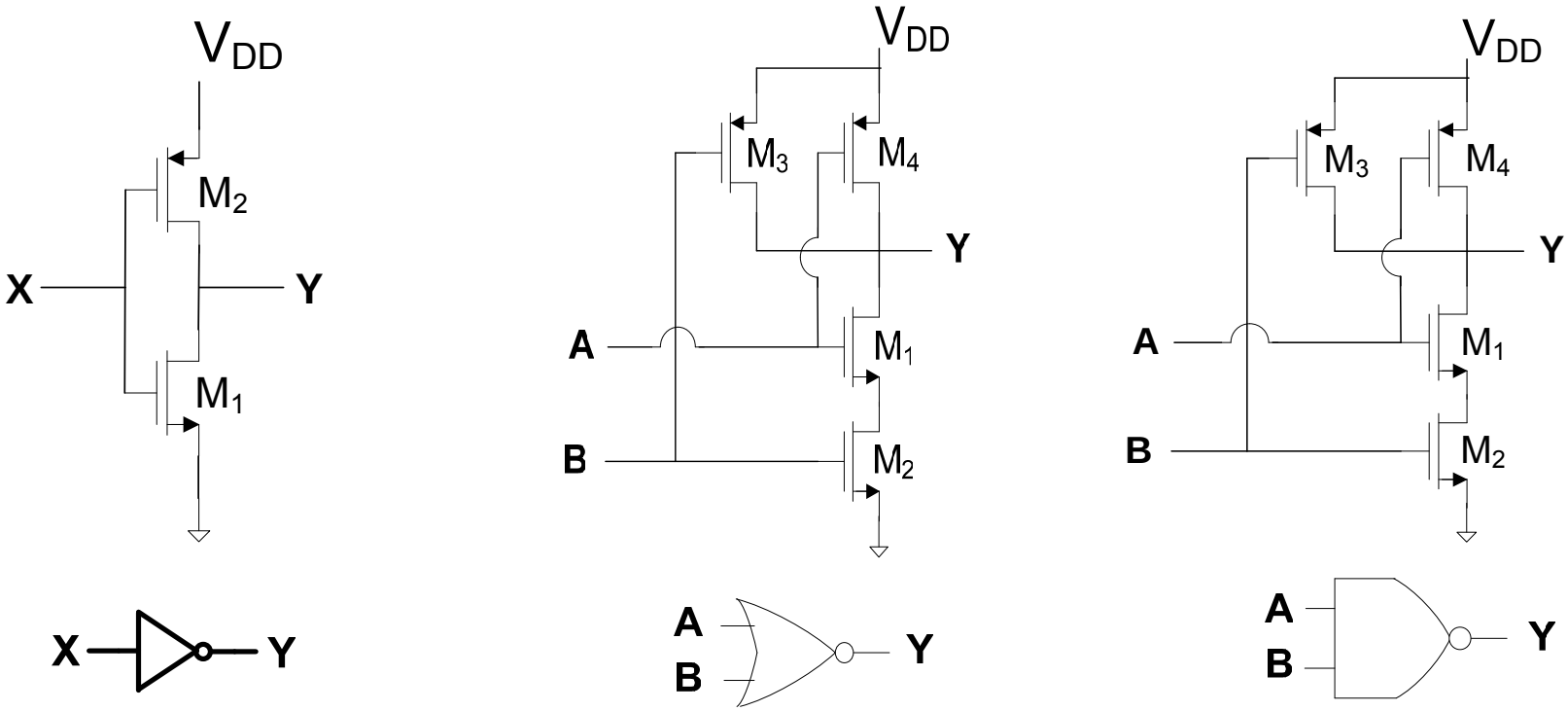
Truth Table

Performs as a 2-input NAND Gate



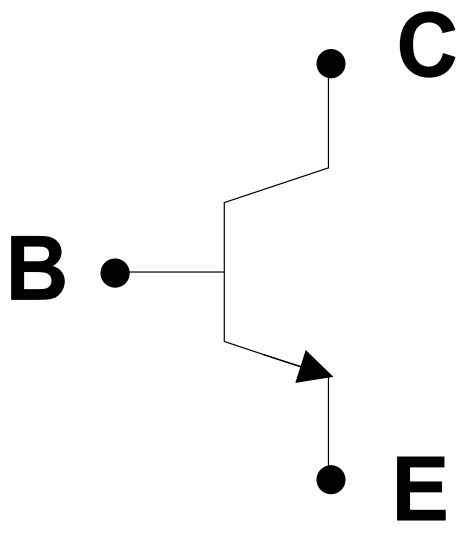
Can be easily extended to an n-input NAND Gate

MOS Transistor Applications (Digital Circuits)



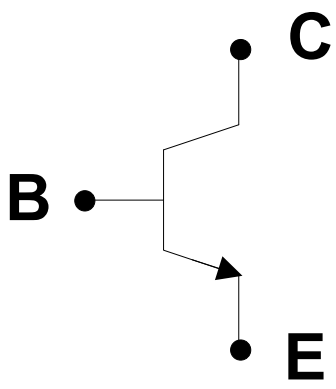
- Termed CMOS Logic
- Widely used in industry today (millions of transistors in many ICs using this logic
- Almost never used as discrete devices

Bipolar Transistor



B: Base
C: Collector
E: Emitter

Bipolar Transistor



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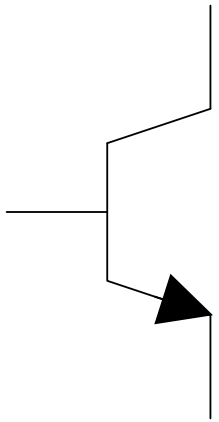
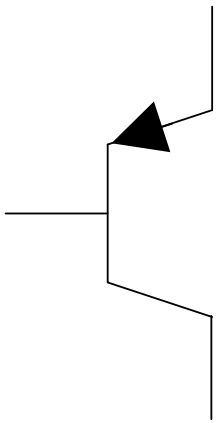
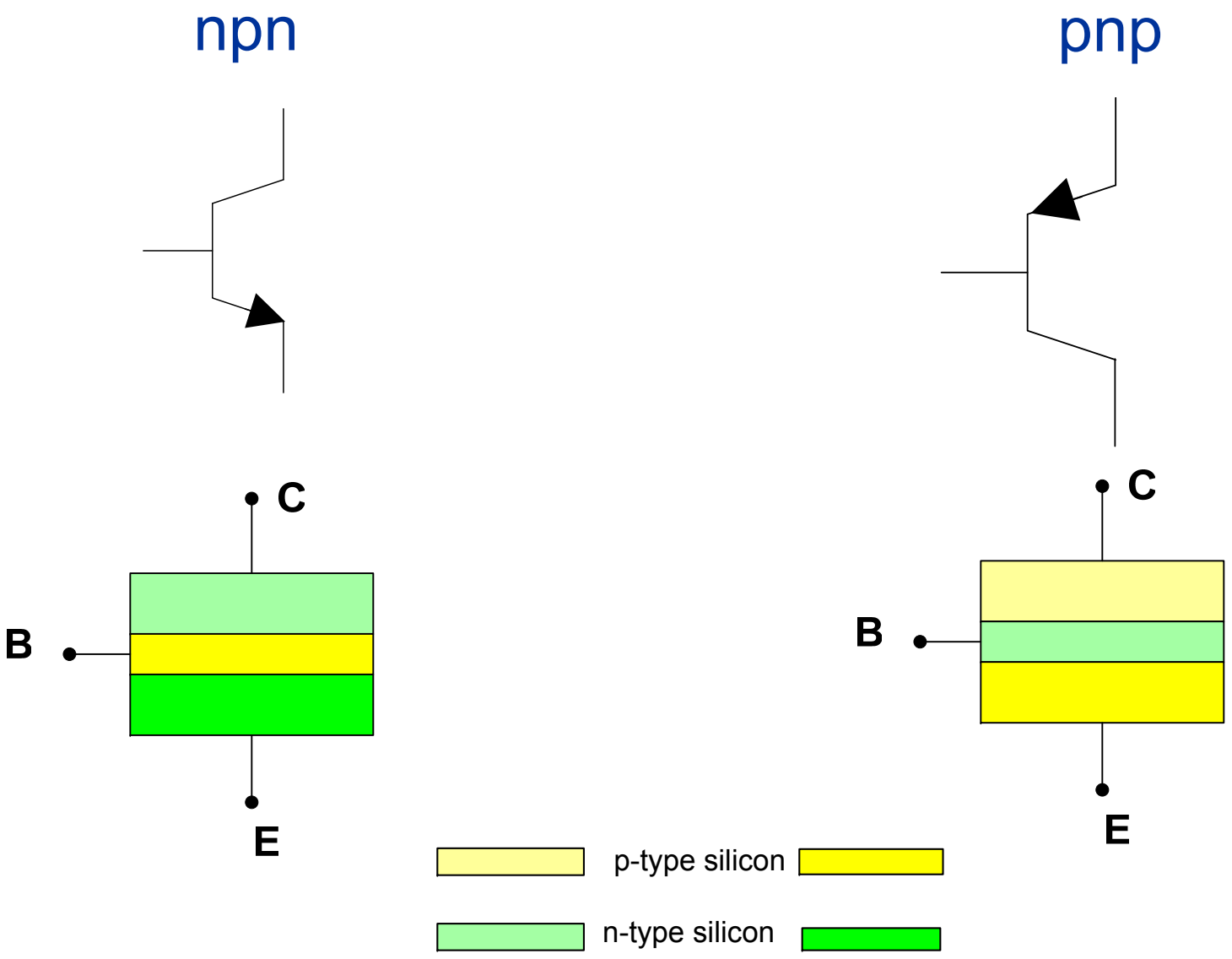


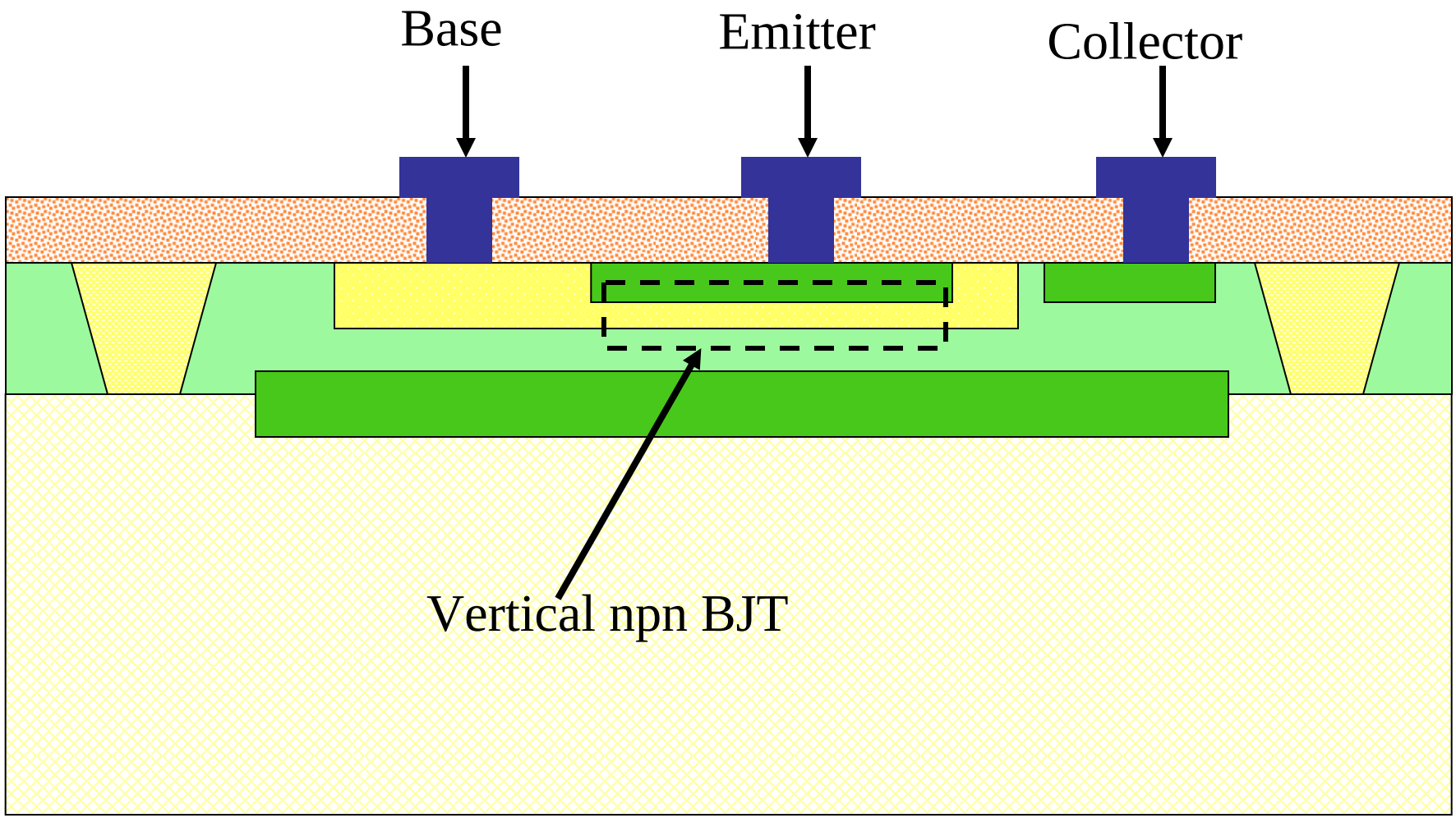
pnp



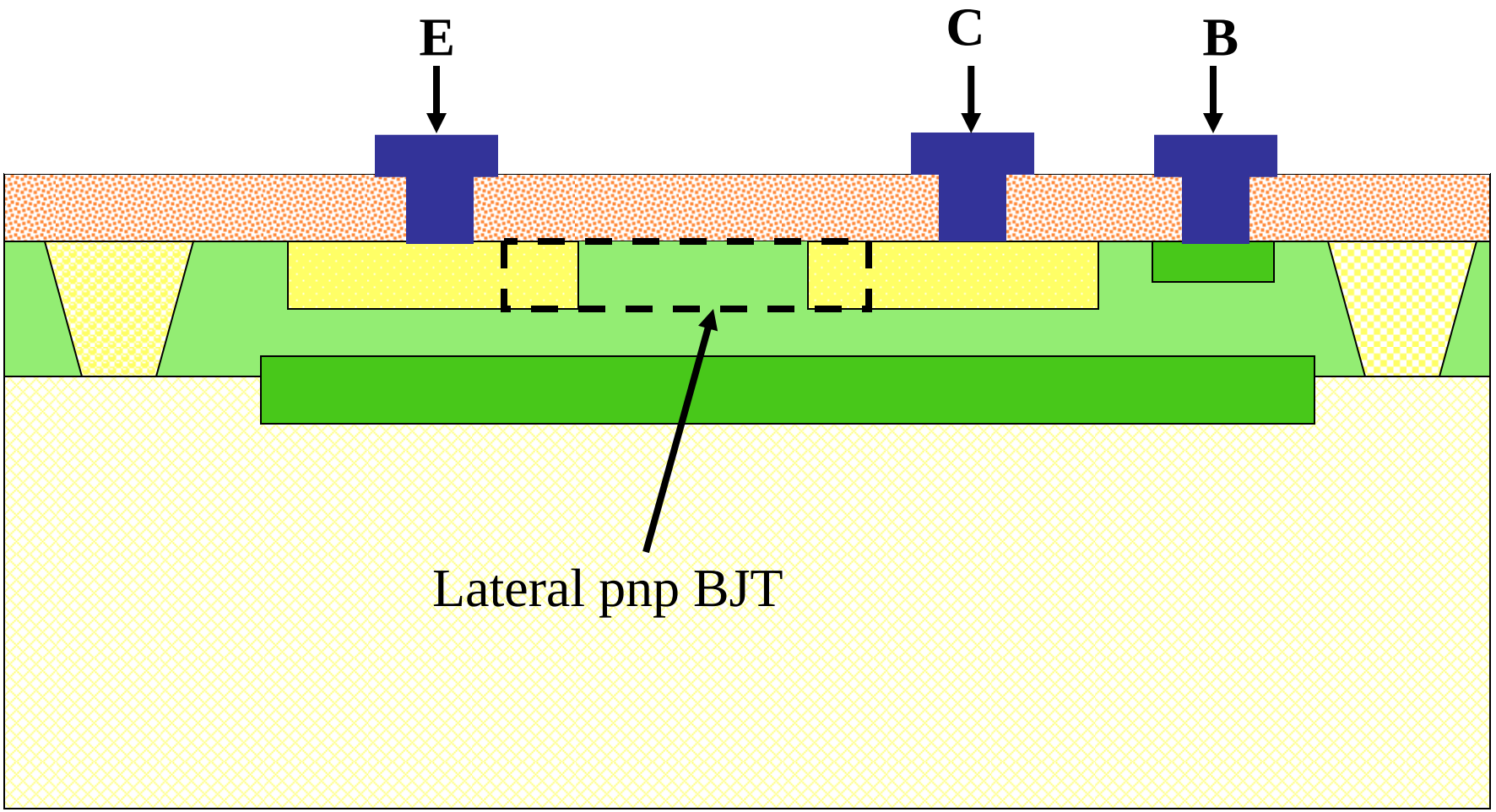
Bipolar Transistor



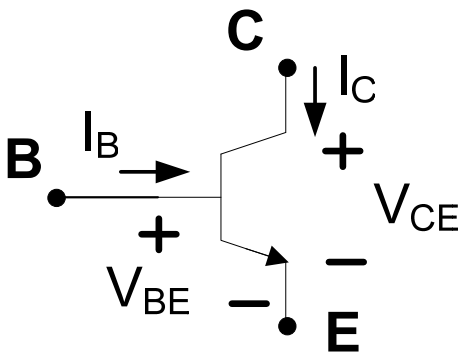
Vertical npn BJT



Lateral pnp BJT



Bipolar Transistor



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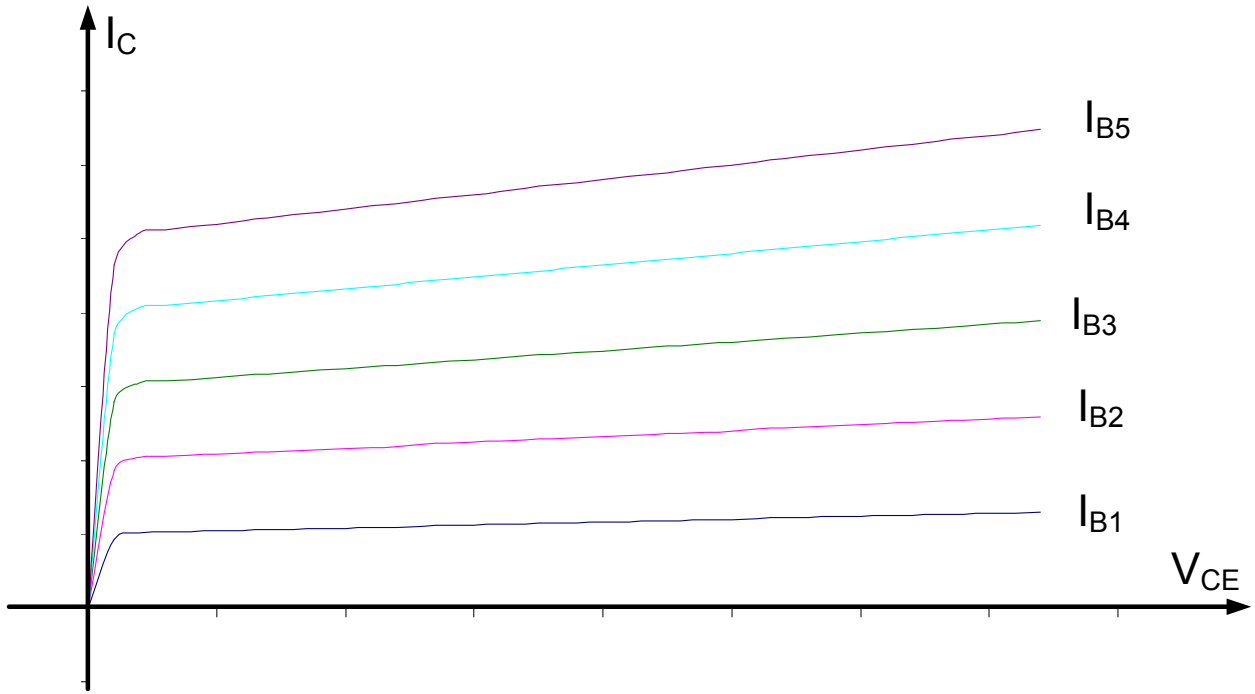
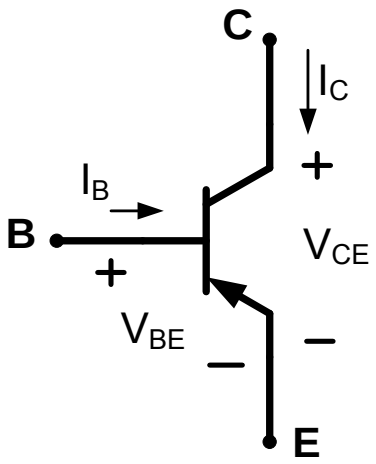


Bipolar Transistor



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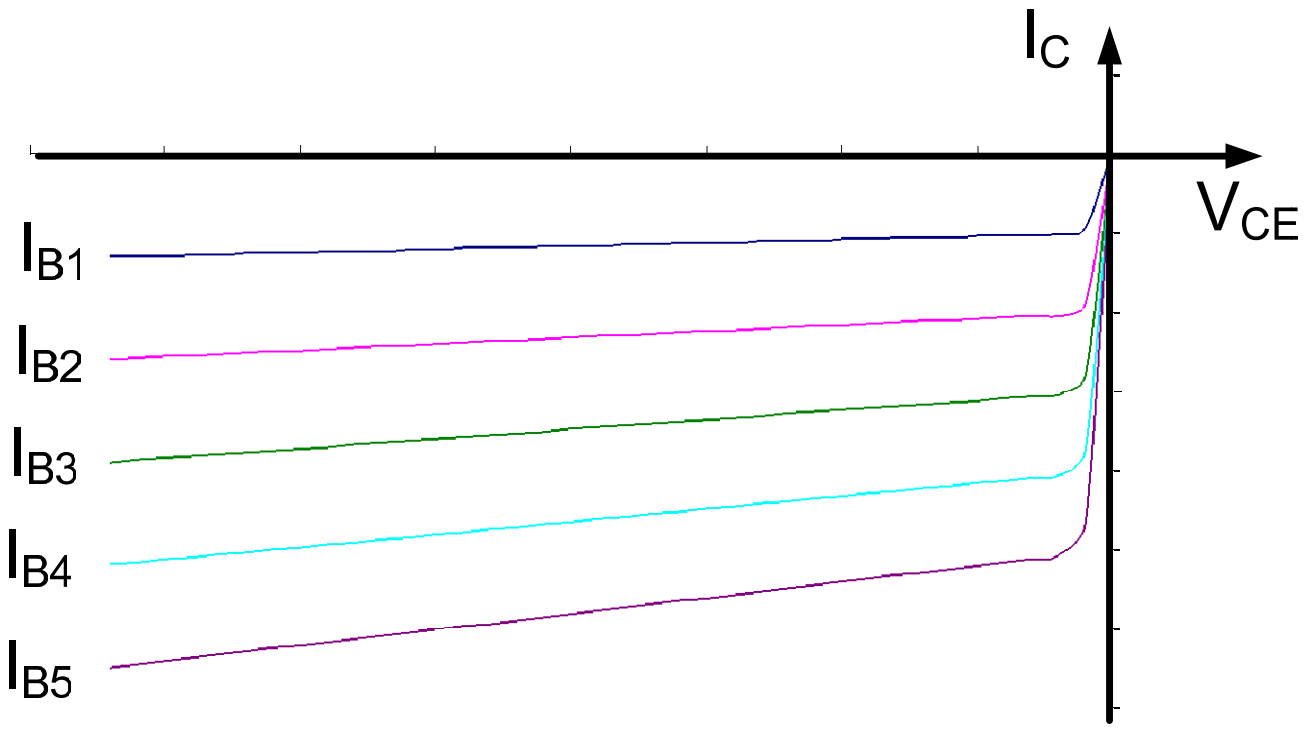
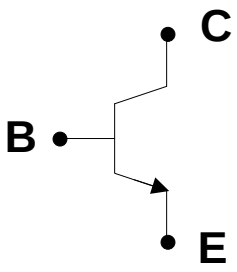
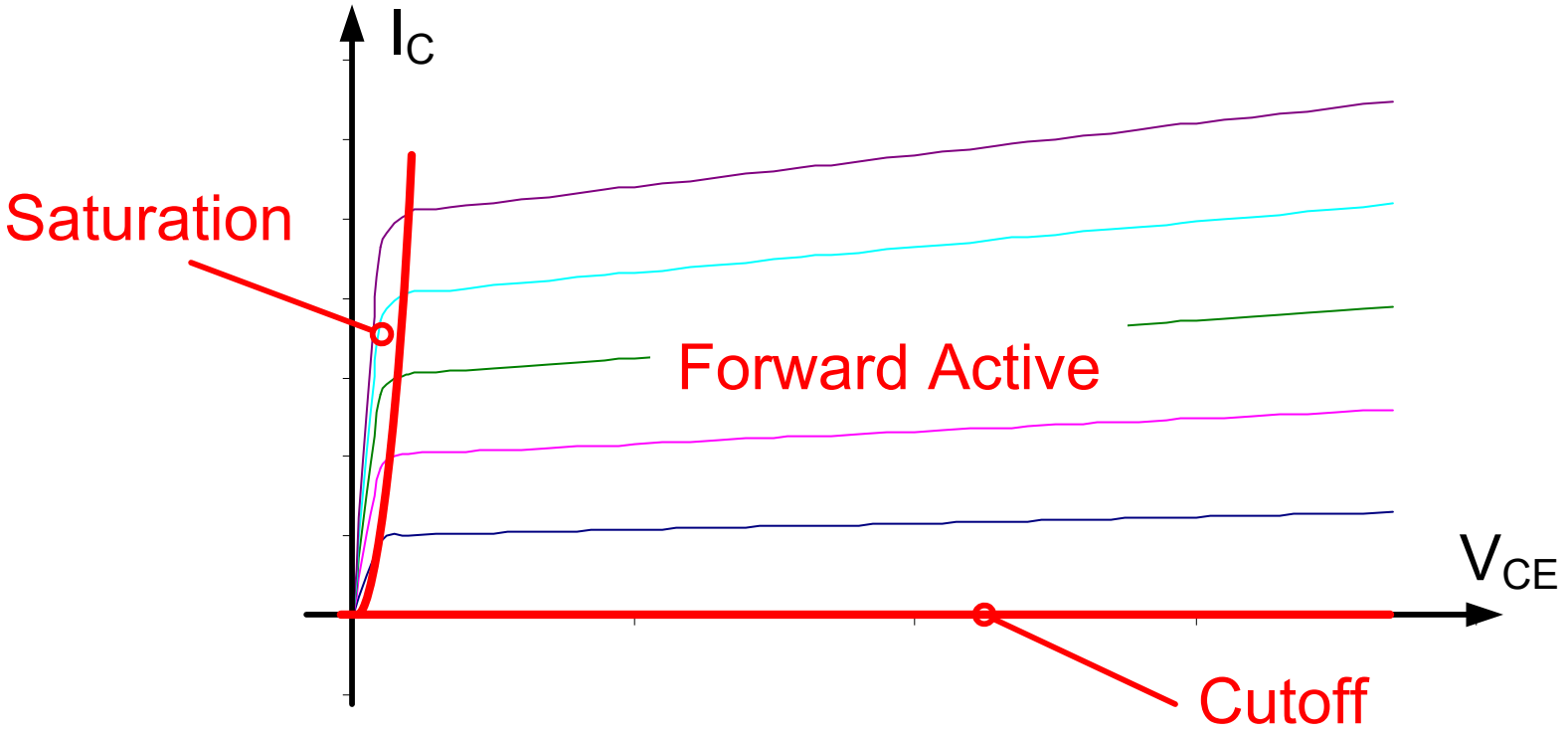
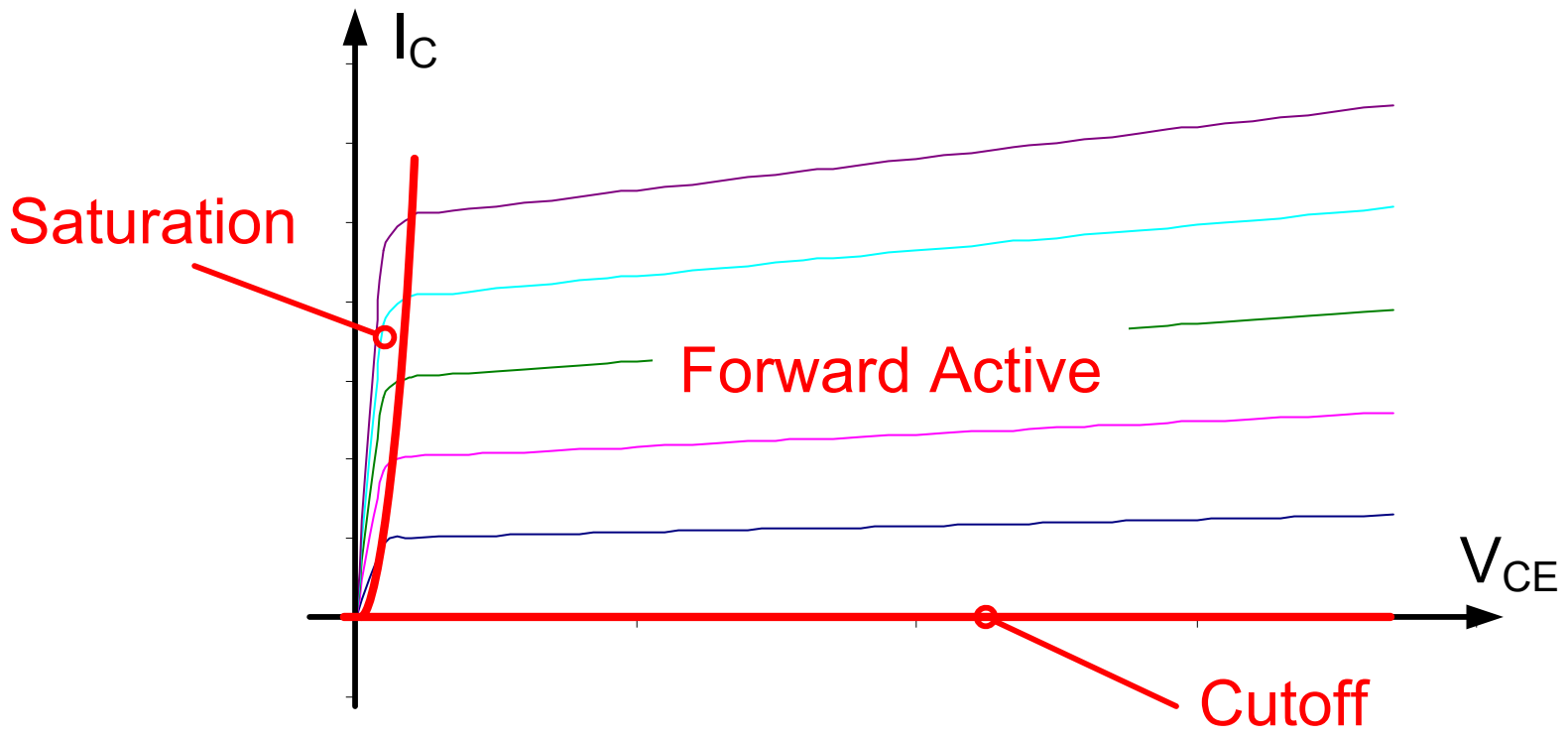


Bipolar Transistor





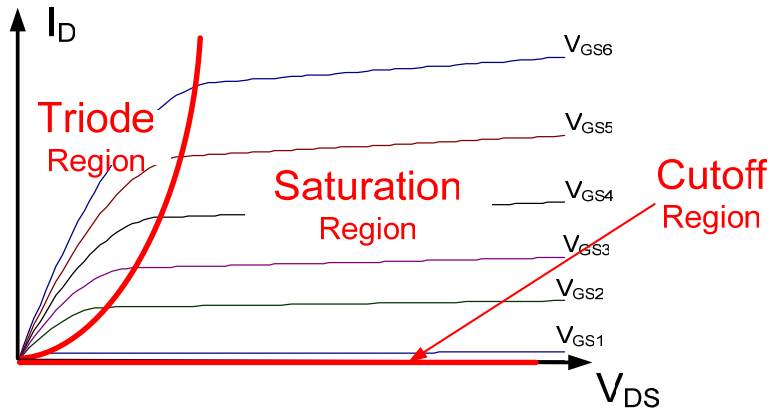
Bipolar Transistor



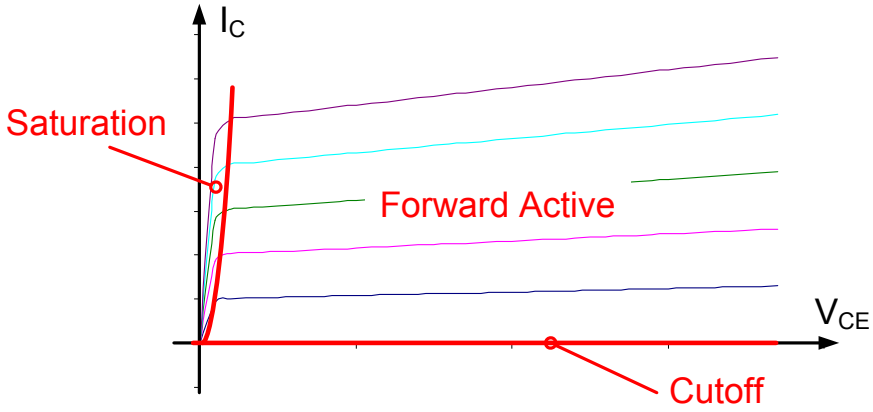
Most analog or linear applications based upon Forward Active region

Most digital applications involve Saturation and Cutoff regions and switching between these regions as the Boolean value changes states

Bipolar and MOS Region Comparisons



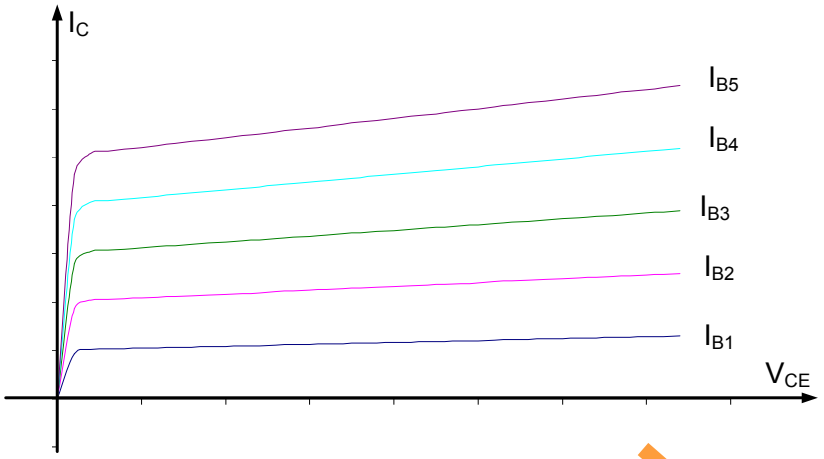
MOSFET

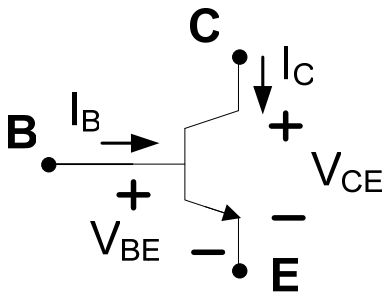


BJT

Cutoff	⟷	Cutoff
Saturation	⟷	Forward Active
Triode	⟷	Saturation

Bipolar Transistor





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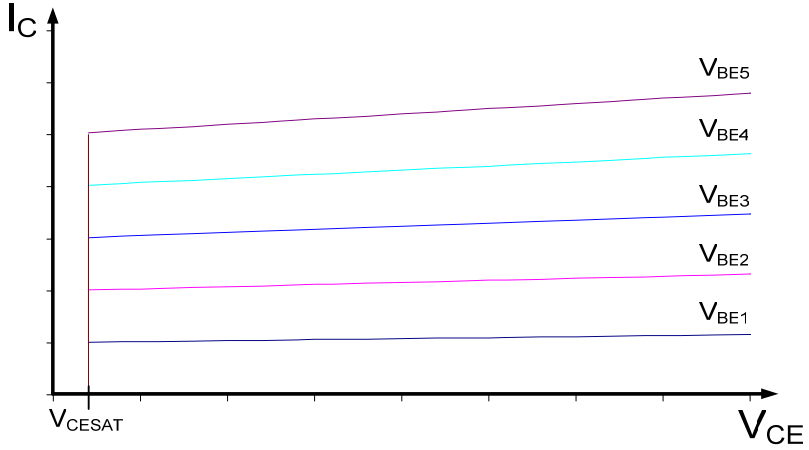


Bipolar Transistor

Multi-Region Model

$$I_C = \beta I_B \left(1 + \frac{V_{CE}}{V_{AF}}\right)$$

$$I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}}$$

$$V_t = \frac{kT}{q}$$

V_{BE}>0.4V

V_{BC}<0

Forward Active

V_{BE}=0.7V
V_{CE}=0.2V

I_C<βI_B

Saturation

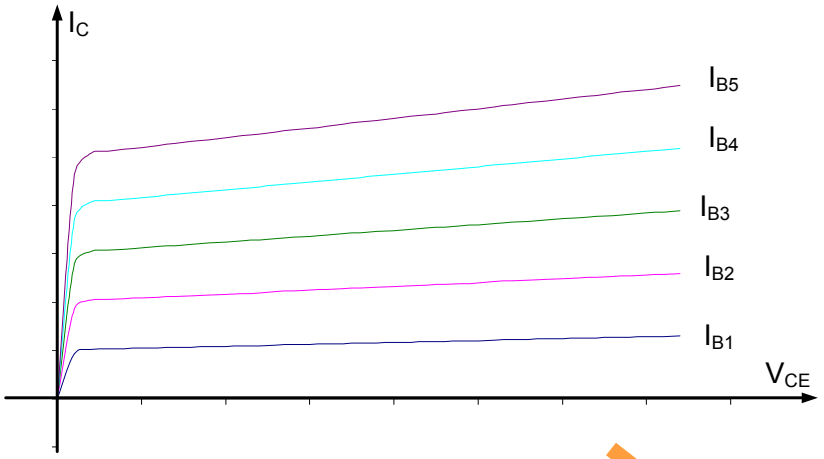
I_C=I_B=0

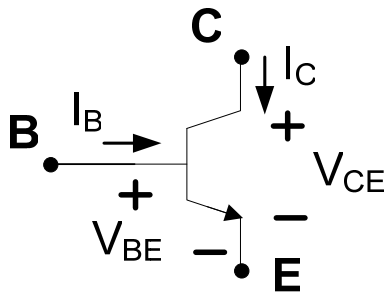
V_{BE}<0

V_{BC}<0

Cutoff

Bipolar Transistor





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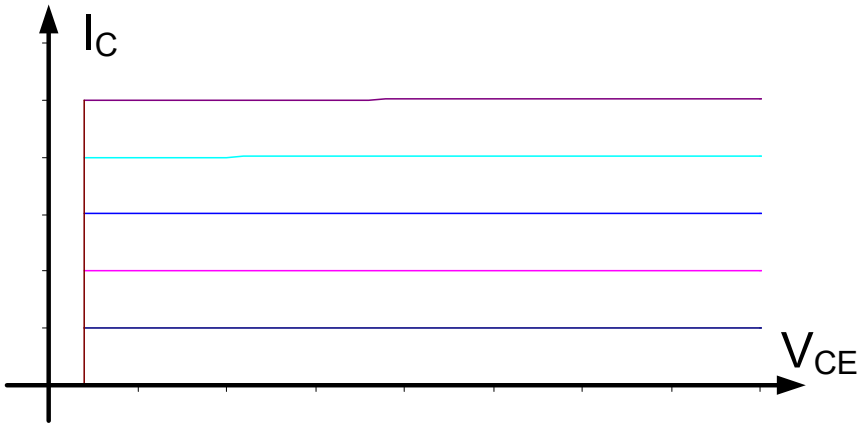

Bipolar Transistor

Simplifier Basic Multi-Region Model

$$I_C = \beta I_B$$

$$I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}}$$

$$V_t = \frac{kT}{q}$$

V_{BE}>0.4V

V_{BC}<0

Forward Active

V_{BE}=0.7V
V_{CE}=0.2V

I_C<βI_B

Saturation

I_C=I_B=0

V_{BE}<0

V_{BC}<0

Cutoff

End of Lecture 31